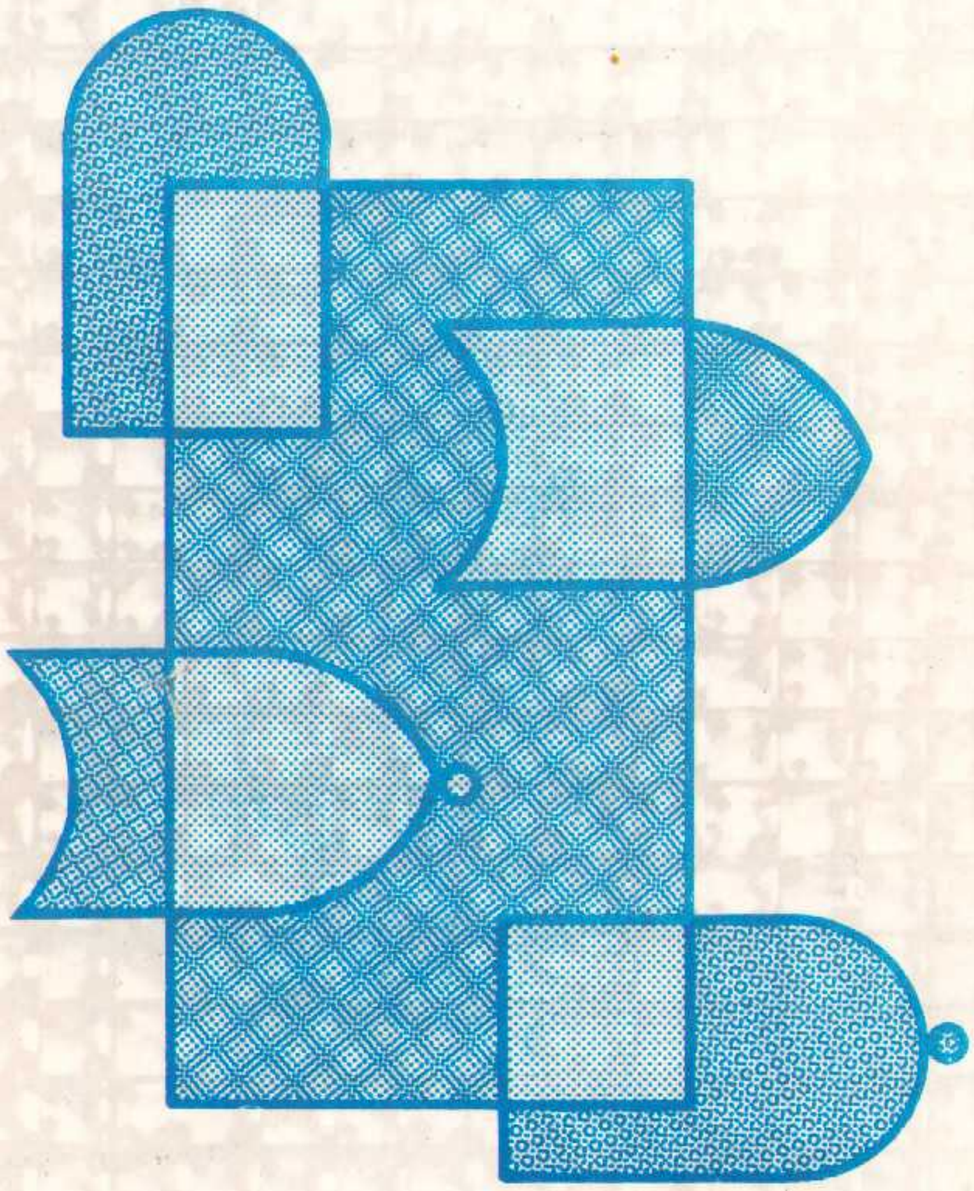
TECHNISCHE DOCUMENTATIE 1970

DEEL 1 2 3 4 5 6 7 8 9 10 11 12

APPLICATIE GEGEVENS TTL



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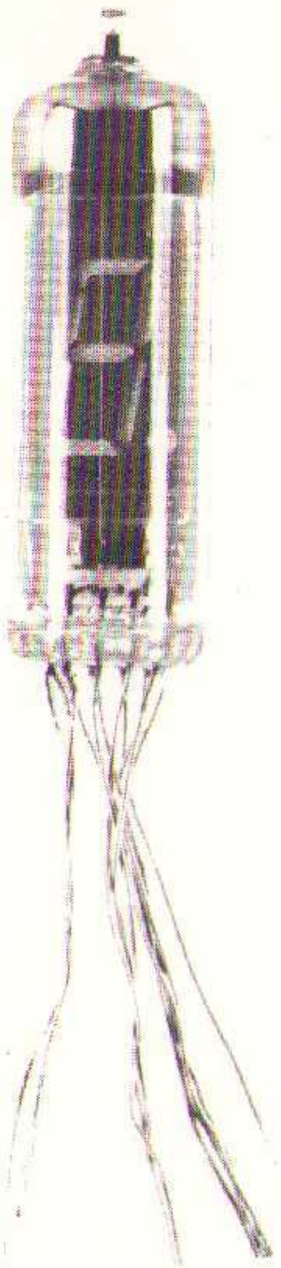
Prijs f 3,90

ITRON Ziffernanzeigeröhre



TYP DG 12 H

- parallaxenfreie Anzeige
- scharfe hellgrüne Zeichen
- geringe Leistungsaufnahme
- niedrige Betriebsspannung

Die Ziffernanzeigeröhre DG 12 H ermöglicht eine sehr wirkungsvolle Darstellung von Zahlen bei äußerst geringer Betriebsspannung und niedriger Leistungsaufnahme. Durch die Anzeige auf einer Ebene sind Helligkeit und Schärfe auch in einem großen Betrachtungswinkel unvermindert gut. Die Zeichen setzen sich aus 7 Segmenten zusammen, die jeweils mit einem Phosphormantel überzogen sind. Sie werden durch die Elektronen erregt, die von der sehr feinen, direkt geheizten Kathode emittiert werden. Die Röhre ist besonders geeignet für dezimal-codierte Geräte, wie Tischrechner, Computeranlagen, Digitalmeßgeräte usw. Es können die Zahlen von 0 bis 9 sowie ein Dezimalpunkt dargestellt werden.

Elektrische Daten:

Allgemeines:	
Kathode	direkt geheizt
Heizstrom	85 mA
Heizspannung bei 85 mA	0,8 V ± 10 %
Helligkeit	80 Foot-Lambert
Farbe der Zeichen	grün
Maximalwerte:	
max. Gleichspannung (Segmente)	25 V–
max. Impulsspannung (Segmente)	55 Vss
min. Gleichspannung (Segmente)	15 V–
max. Gleichspannung (Gitter)	25 V–
max. Impulsspannung (Gitter)	55 Vss
min. Gleichspannung (Gitter)	15 V–
max. Heizstrom	89 mA
Normalwerte:	
Kathodenstrom (bei 20 V Segment u. Gittersp.)	5 mA
Segmentstrom	1 mA
Strom durch Dezimalpunkt	0,1 mA

Mechanische Daten:

Gesamtlänge	45 mm
Durchmesser	Ø 13,5 mm
Ziffernhöhe	12,2 mm
Ziffernbreite	8,3 mm
Dezimalpunkt	Ø 1,8 mm
Gewicht	6 g
Einbaulage	beliebig
Betrachtungswinkel	ca. 90°
Umgebungstemperatur	–10 bis +70° C

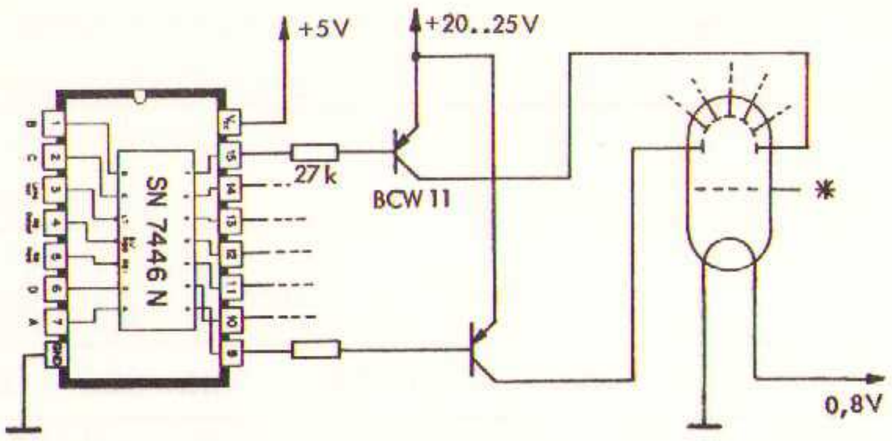
Typische Betriebsdaten:

Betriebsart	Gleichspg.	Impulsbetrieb (max. 55 Vss) Impuls-Pausenverhältnis 1:4	1:8	1:16	1:20
Heizung	0,8 V	0,8 V	0,8 V	0,8 V	0,8 V
Segment und Gitter	20 V	30 Vss	40 Vss	50 Vss	55 Vss
Gitterabschaltspg.	–4 V	–4 Vss	–4 Vss	–4 Vss	–4 Vss
Segment „aus"	0 V	0 V	0 V	0 V	0 V

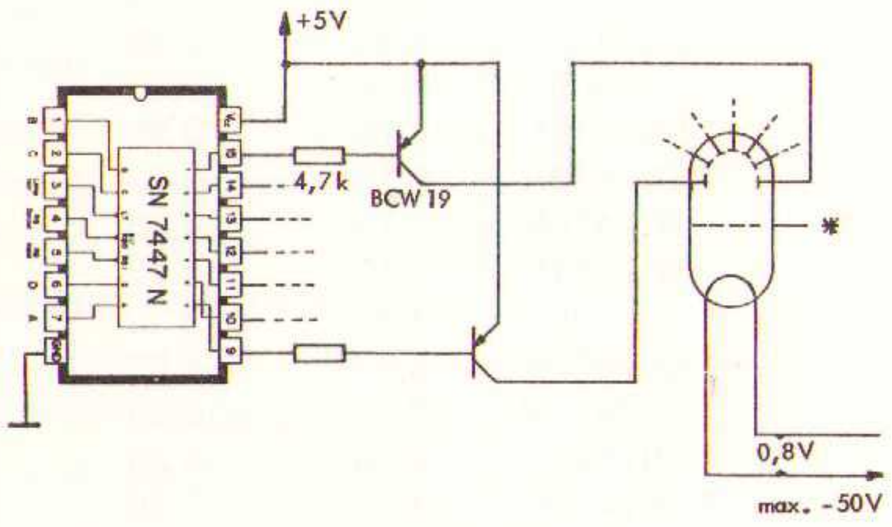
ITRON Ziffernanzeigeröhre

Schaltungsbeispiele:

DC-Betrieb:

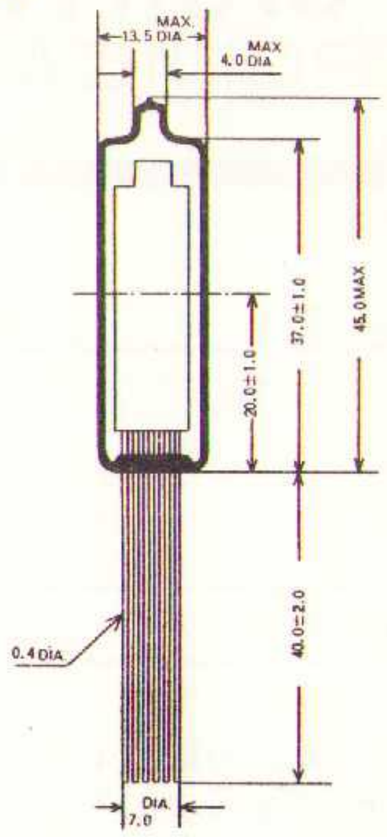


Impulsbetrieb:

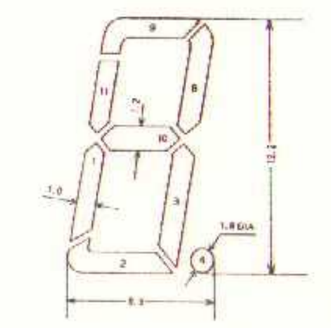


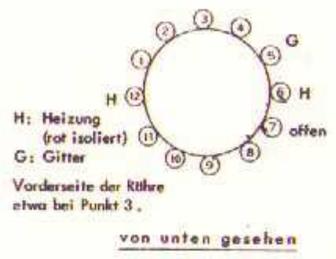
* Gitteranschlüss
(voordeel van deze aansluiting zal in een komende documentatie worden besproken!)

Abmessungen:



Anschlüsse:





Anschlüsse:

Treiber	Röhre
SN 74..	DG 12 H
e	1
d	2
c	3
	4 Dez.punkt
	5 Gitter
	6 Heizung
	7 offen
b	8
a	9
g	10
f	11
	12 Heizng.

Ziffern (Originalgröße):

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TTL

20 juli 1970 — **Prijs in Nederlandse guldens Exclusief B.T.W.**

Omschrijving	Type	1 - 24	25 - 99	100 - 499
Quadruple 2-Input Positive NAND Gate	* SN7400N	4,28	3,30	2,78
Quadruple 2-Input Positive NAND Gate (Open Collector Output)	SN7401N	4,28	3,30	2,78
Quadruple 2-Input Positive NOR Gate	* SN7402N	4,28	3,30	2,78
Quadruple 2-Input Positive NAND Gate (Open Collector Output)	SN7403N	4,28	3,30	2,78
Hex Inverter	* SN7404N	5,24	4,04	3,40
Hex Inverter	SN7405N	5,24	4,04	3,40
Hex Inverter Buffer/Driver (30 Volt)	SN7406N	8,92	6,88	5,79
Hex Buffer/Driver (30 Volt)	SN7407N	8,92	6,88	5,79
Quadruple 2-Input Positive AND Gate	* SN7408N	4,36	3,36	2,83
Quadruple 2-Input Positive AND Gate	SN7409N	4,36	3,36	2,83
Triple 3-Input Positive NAND Gate	* SN7410N	4,28	3,30	2,78
Dual Schmitt Trigger	* SN7413N	6,13	4,73	3,98
Hex Inverter Buffer/Driver (15 Volt)	SN7416N	6,13	4,73	3,98
Hex Buffer/Driver (15 Volt)	SN7417N	6,13	4,73	3,98
Dual 4-Input Positive NAND Gate	* SN7420N	4,28	3,30	2,78
Dual 4-Input Positive NOR Gate (Expandable)	SN7423N	8,92	6,88	5,79
Dual 4-Input Positive NOR Gate	SN7425N	8,21	6,33	5,33
Quadruple 2-Input Positive NAND Gate (30 Volt)	* SN7426N	4,36	3,36	2,83
8-Input Positive NAND Gate	* SN7430N	4,28	3,30	2,78
Quadruple 2-Input Positive NAND Buffer	SN7437N	8,40	6,47	5,45
Quadruple 2-Input Positive NAND Buffer (Open Collector)	SN7438N	8,40	6,47	5,45
Dual 4-Input Positive NAND Buffer	* SN7440N	4,53	3,49	2,94
BCD-to-Decimal Decoder/Driver (Nixie Tube)	* SN7441AN	26,03	20,07	16,89
√ BCD-to-Decimal Decoder	* SN7442N	19,93	15,36	12,93
Excess-3-to-Decimal Decoder	SN7443N	25,73	19,82	16,68
Excess-3 Gray-to-Decimal Decoder	SN7444N	25,73	19,82	16,68
BCD-to-Decimal Decoder/Driver (80 mA sink)	SN7445N	39,34	30,33	25,53
BCD-to-Seven Segment Decoder/Driver (20 mA sink)	* SN7446N	32,53	25,08	21,11
BCD-to-Seven Segment Decoder/Driver (20 mA sink)	SN7447N	30,03	23,15	19,49
BCD-to-Seven Segment Decoder/Driver (10 mA sink)	SN7448N	25,73	19,82	16,68
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	* SN7450N	4,28	3,30	2,78
Dual 2-Wide 2-Input AND-OR-INVERT Gate	* SN7451N	4,28	3,30	2,78
Expandable 4-Wide 2-Input AND-OR-INVERT Gate	* SN7453N	4,28	3,30	2,78
4-Wide 2-Input AND-OR-INVERT Gate	* SN7454N	4,28	3,30	2,78
Dual 4-Input Expander	* SN7460N	4,28	3,30	2,78
J-K Flip-Flop	* SN7470N	7,69	5,93	4,99
J-K Master-Slave Flip-Flop	* SN7472N	6,06	4,67	3,93
Dual J-K Master-Slave Flip-Flop	* SN7473N	9,92	7,65	6,44
Dual D-Type Edge-Triggered Flip-Flop	* SN7474N	8,85	6,82	5,74
Quadruple Bistable Latch	* SN7475N	13,96	10,76	9,06

* Voorraad magazijn Rotterdam, overige typen op bestelling leverbaar.

PRIJSVERANDERINGEN ZIJN STRIKT VOORBEHOUDEN !!!!

Omschrijving		Type	1 - 24	25 - 99	100 - 499
Dual J-K Master-Slave Flip-Flop with Preset and Clear	*	SN7476N	10,37	8,00	6,73
Gated Full Adder	*	SN7480N	13,50	10,41	8,76
16-Bit Active Element Memory		SN7481N	22,04	16,99	14,30
2-Bit Binary Full Adder	*	SN7482N	20,00	15,42	12,98
4-Bit Binary Full Adder	*	SN7483N	30,03	23,15	19,49
16-Bit Active Element Memory (Gated Write Inputs)		SN7484N	22,04	16,99	14,30
4-Bit Magnitude Comparator		SN7485N	30,42	23,45	19,74
Quadruple 2-Input exclusive OR Gate	*	SN7486N	9,05	6,97	5,87
Decade Counter	*	SN7490N	16,30	12,57	10,58
8-Bit Shift Register	*	SN7491AN	22,04	16,99	14,30
Divide-by-Twelve Counter	*	SN7492N	17,26	13,31	11,20
4-Bit Binary Counter	*	SN7493N	17,26	13,31	11,20
4-Bit Shift Register	*	SN7494N	20,93	16,13	13,58
4-Bit Right/Left Shift Register	*	SN7495N	20,93	16,13	13,58
5-Bit Shift Register	*	SN7496N	25,10	19,35	16,29
Dual Quadruple Bistable Latch	*	SN74100N	33,67	25,96	21,85
Dual J-K Master-Slave Flip-Flop		SN74107N	9,92	7,65	6,44
High Speed J-K Flip-Flop		SN74110N	9,35	7,21	6,07
6-Bit Latch		SN74118N	17,47	13,47	11,34
6-Bit Latch		SN74119N	22,45	17,31	14,57
Monostable	*	SN74121N	10,93	8,42	7,09
Retriggable O.S. with Clear		SN74122N	15,49	11,94	10,05
BCD-to-Decimal Decoder/Driver (80 mA sink)		SN74145N	26,24	20,23	17,03
16-Bits Data Selector		SN74150N	43,04	33,18	27,93
8-Bits Data Selector (with Strobe)		SN74151N	16,80	12,95	10,90
Dual 4-Line-to-1-Line Data Selector/Multiplexer	*	SN74153N	15,21	11,73	9,87
4-Line-to-16-Line Decoder/Demultiplexer		SN74154N	29,31	22,60	19,02
Dual 2 to 4 Line Decoder Demultiplexer	*	SN74155N	14,16	10,92	9,19
Dual 2 to 4 Line Decoder Demultiplexer		SN74156N	13,92	10,73	9,03
8-Bit Parallel-Out Serial Shift Register		SN74164N	37,57	28,96	24,83
Parallel-Load 8-Bit Shift Register		SN74165N	43,81	33,77	28,43
Synchroom Parallel-Load 8-Bit Shift Register		SN74166N	37,57	28,96	24,83
4-by-4 Register File		SN74170N	36,78	28,36	23,87
8-Bit Odd/Even Parity Generator/Checker		SN74180N	20,99	16,18	13,62
4-Bit Arithmetic Logic Unit		SN74181N	79,20	61,06	51,40
Look-Ahead Carry Generator		SN74182N	15,76	12,98	10,93
Binary BCD Decoder		SN74185N	60,58	46,70	39,31
Synchroon Decade Up/Down Counter		SN74190N	56,12	43,27	36,42
Synchroon 4-Bits Up/Down Counter		SN74191N	56,12	43,27	36,42
Synchroon Decade Up/Down Counter	*	SN74192N	42,32	32,62	27,46
Synchroon 4-Bits Up/Down Counter		SN74193N	42,32	32,62	27,46
50-mHz Presettable Decade Counter		SN74196N	22,31	17,20	14,48
50-mHz Presettable 4-Bit Binary Counter		SN74197N	22,31	17,20	14,48
8-Bit Parallel-Access, Left-Shift Right-Shift Register		SN74198N	50,38	38,84	32,69
8-Bit Parallel-Access Shift Register		SN74199N	50,38	38,84	32,69

* Voorraad magazijn Rotterdam, overige typen op bestelling leverbaar.

PRIJSVERANDERINGEN ZIJN STRIKT VOORBEHOUDEN !!!!

LOGIC DESIGN WITH SERIES 54/74 GATES

Ronald Crowe and Louis Delhom

INTRODUCTION

The two basic logic functions of OR and AND are often used in computer and control systems. The simplest form for each of these functions is shown below

OR: Output Y = A + B (1)

AND: Output Y = AB (2)

Either of these expressions may be expanded by increasing the number of terms. In addition, the OR and AND functions may be combined in one expression; two examples are

OR-AND: Output Y = (A+B+C) (D+E+F) (3)

AND-OR: Output Y = ABC + DEF (4)

Equations (1) through (4) are equations of Boolean algebra, and are referred to as *logic* expressions. The binary number system, consisting of the binary digits 1 and 0, is used for Boolean algebra. Hence, any term in the above expressions may be replaced by 1 or 0. The output Y for any expression will be either 1 or 0, depending upon whether the right side of the equation is *true* or *false*, respectively, for the particular values of variables.

Various combinations of diode AND and OR gates can be used to implement the above Boolean expressions. For instance, the diode-logic circuit which satisfies eq. (3) is shown in Figure 1. Input-signal levels are shifted and attenuated in passing through this circuit; consequently, diode logic gates generally cannot be cascaded beyond two or three stages.

An inverter stage may be added to the output of a diode logic gate to regenerate, or shape, the output signal. This permits an indefinite number of gates to be cascaded. The output signal from the inverter stage is the complement, or inverse, of the output signal from the diode gate. The AND gate becomes a NAND gate, and the OR gate is changed to a NOR gate. This is of advantage when it is desired to complement an input signal; one disadvantage is that greater attention must now be given to the logical output from the circuit. As an example of the difficulty which arises with NAND gates, consider that it is desired to implement eq. (2) with NAND logic. If inputs A and B are applied to the NAND gate, the output will be $\overline{AB}$. A second NAND gate can be used to invert this term and provide AB. Two NAND gates are now required, whereas a single AND gate would suffice. However, it may be possible to obtain AB by use of a single NOR gate; this is described later.

Because integrated circuits offer advantages in cost, reliability, and space, it is advantageous to use these elements in logic circuits. Integrated circuits are generally available only in the NAND and NOR forms. For these reasons, this report describes methods of implementing logic functions with NAND and NOR gates; various design techniques are presented which minimize the number of gates. Specific circuit configurations are given for gates of the TTL 54/74 series.

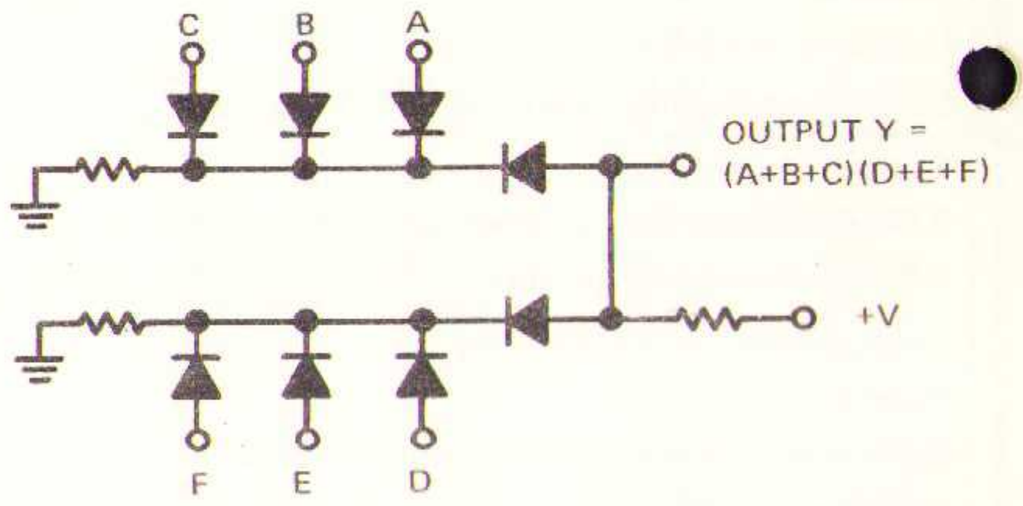


FIGURE 1. Diode-Logic Circuit to Perform Y = (A + B + C) (D + E + F)

DESCRIPTION OF SERIES 54/74 GATES

Series 54 and series 74 are the designations for two families of digital integrated circuits. The same basic gate circuits are available in either series; however, series 54 devices operate over the military temperature range of -55°C to 125°C, whereas series 74 devices operate only over the industrial temperature range of 0°C to 70°C. Insofar as the logic function of a gate is concerned, it is immaterial whether the series 54 or series 74 devices are considered. Hence the designation series 54/74 is used to mean either series 54 or series 74 circuits. As is the case for all integrated circuits manufactured by Texas Instruments, device numbers in these two series are prefixed with the letters SN.

Before going on to a detailed description of series 54/74 gates, let us discuss briefly the terms *positive logic* and *negative logic*. Positive logic assigns binary 1 to the most positive signal level and binary 0 to the most negative signal level. For negative logic, the most negative signal level is regarded as binary 1, and the most positive signal level is considered to be binary 0. The NAND and NOR gates for positive logic become NOR and NAND gates, respectively, for negative logic. Positive logic is more widely used than negative logic; consequently the positive-logic designation for series 54/74 gates is used throughout the remainder of this report.

Figure 2(a) shows the most common type of series 54/74 TTL NAND gate. The circuit has two input emitters which

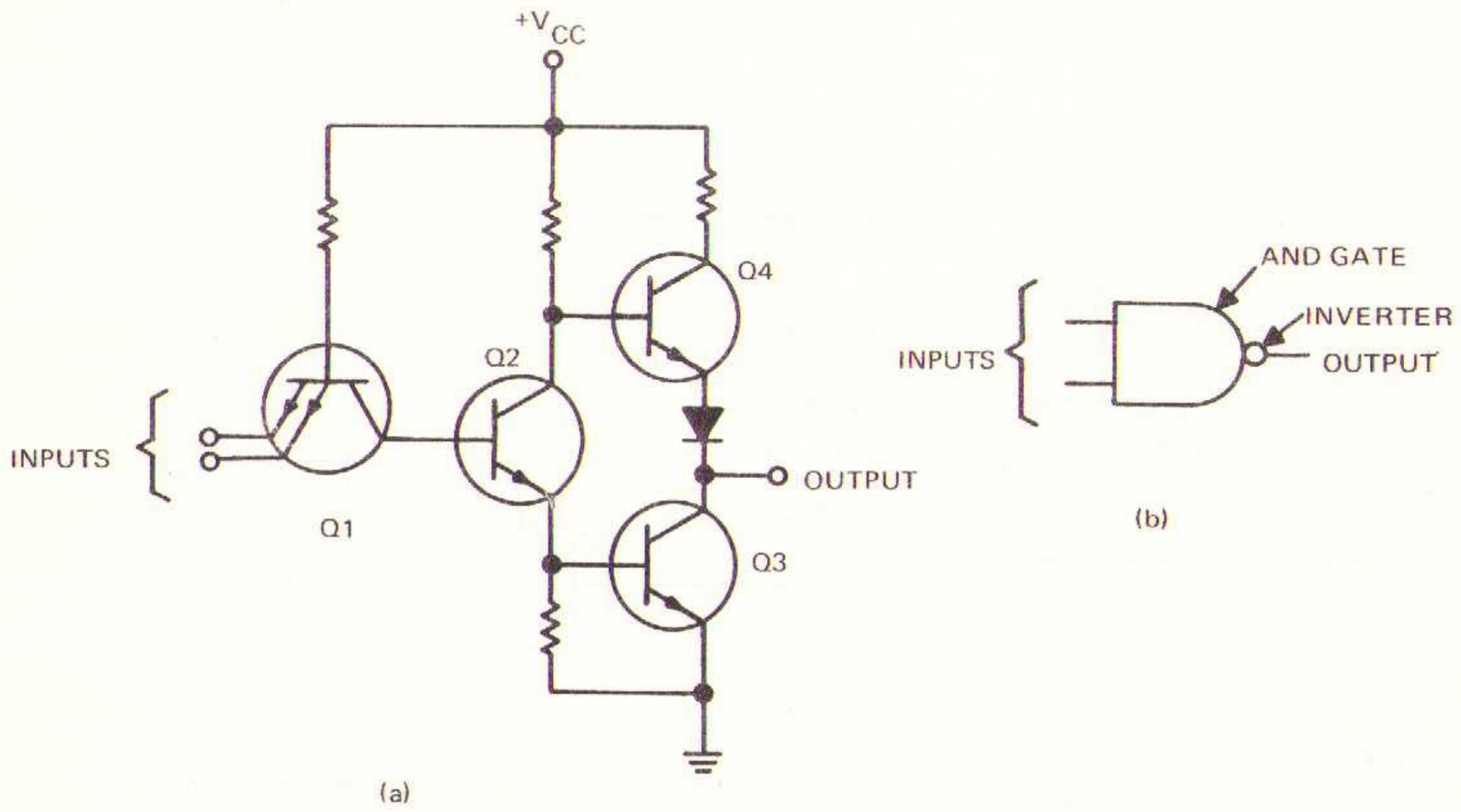


FIGURE 2. Circuit and Symbol for Series 54/74 NAND Gate

are driven by input signals. If either emitter is at ground potential, the output signal is close to the V_{CC} level. When both emitters are open-circuited or at a positive potential greater than 2.0 volts, the output signal is close to ground potential. The logic diagram for this circuit is given in Figure 2(b); two logic circuits are shown – an AND gate and an inverter.

Transistors Q_3 and Q_4 in Figure 2(a) provide a positive driving action during both the low and high output states; load current is *sinked* by Q_3 and is *sourced* by Q_4. These two devices are connected in the "totem-pole" configuration.

The SN5401/7401 NAND gate does not have the above "totem-pole" output stage; only a single output transistor is used. This permits two or more output collectors to be tied together as shown in Figure 3; an external resistor connected to V_{CC} provides a positive output signal when both output transistors are at cutoff. The logic expression for these two gates is

$$\text{OUTPUT } Y = \overline{AB + CD} \tag{5}$$

A total of seven gates may be wired in the above manner; this expands eq. (5) to seven OR'ed terms. The fan-out capability of a single SN5401/7401 gate is 10. When two or more of these gates are connected as in Figure 3, the fan-out capability of the combination is reduced; the maximum permissible fan-out depends upon the number of parallel gates and the value of load resistance.

A NOR-type series 54/74 gate is shown in Figure 4(a). The output signal is positive only when both input emitters are

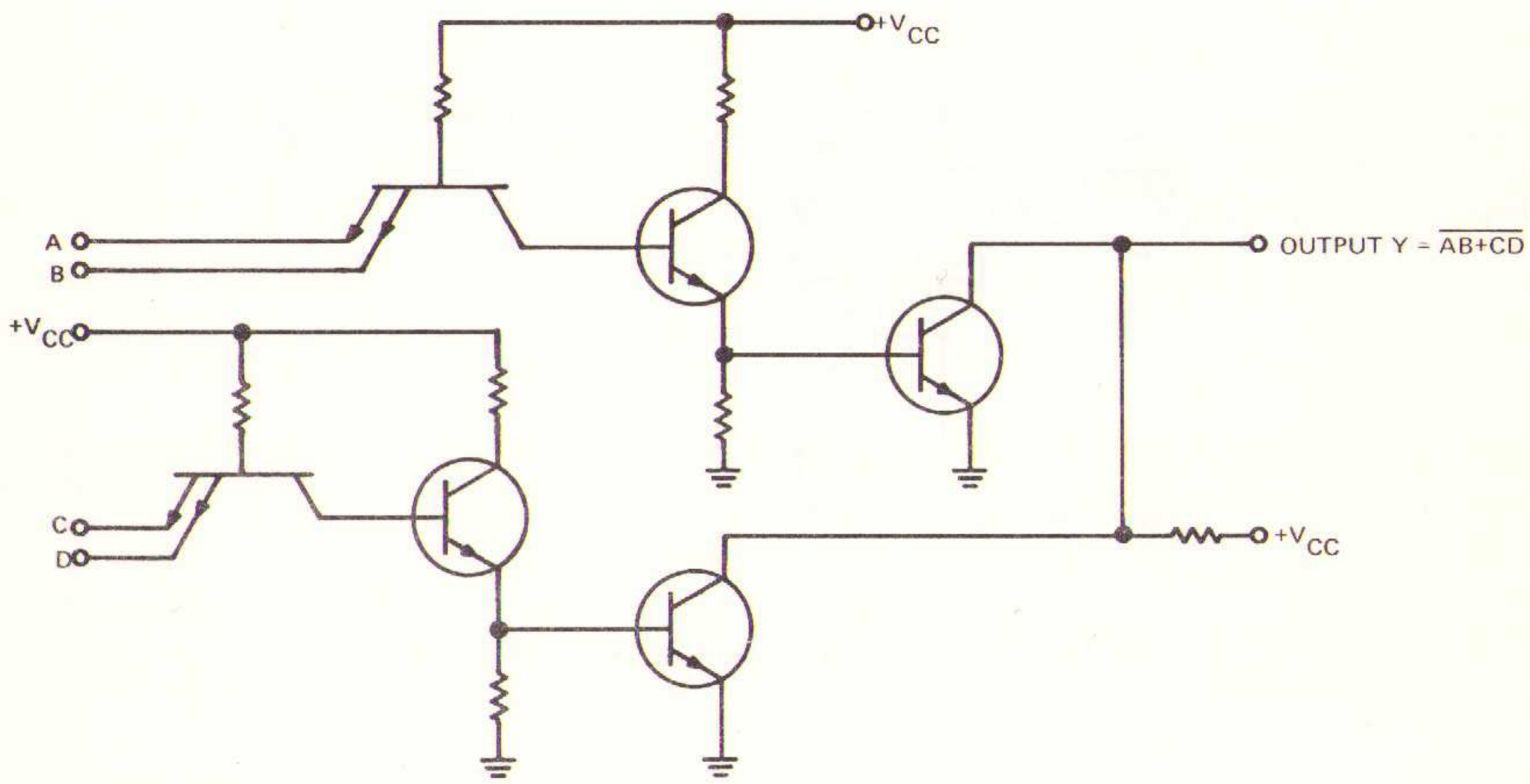


FIGURE 3. Circuit for OR Function Using SN7401 NAND Gates: $Y = \overline{AB + CD}$

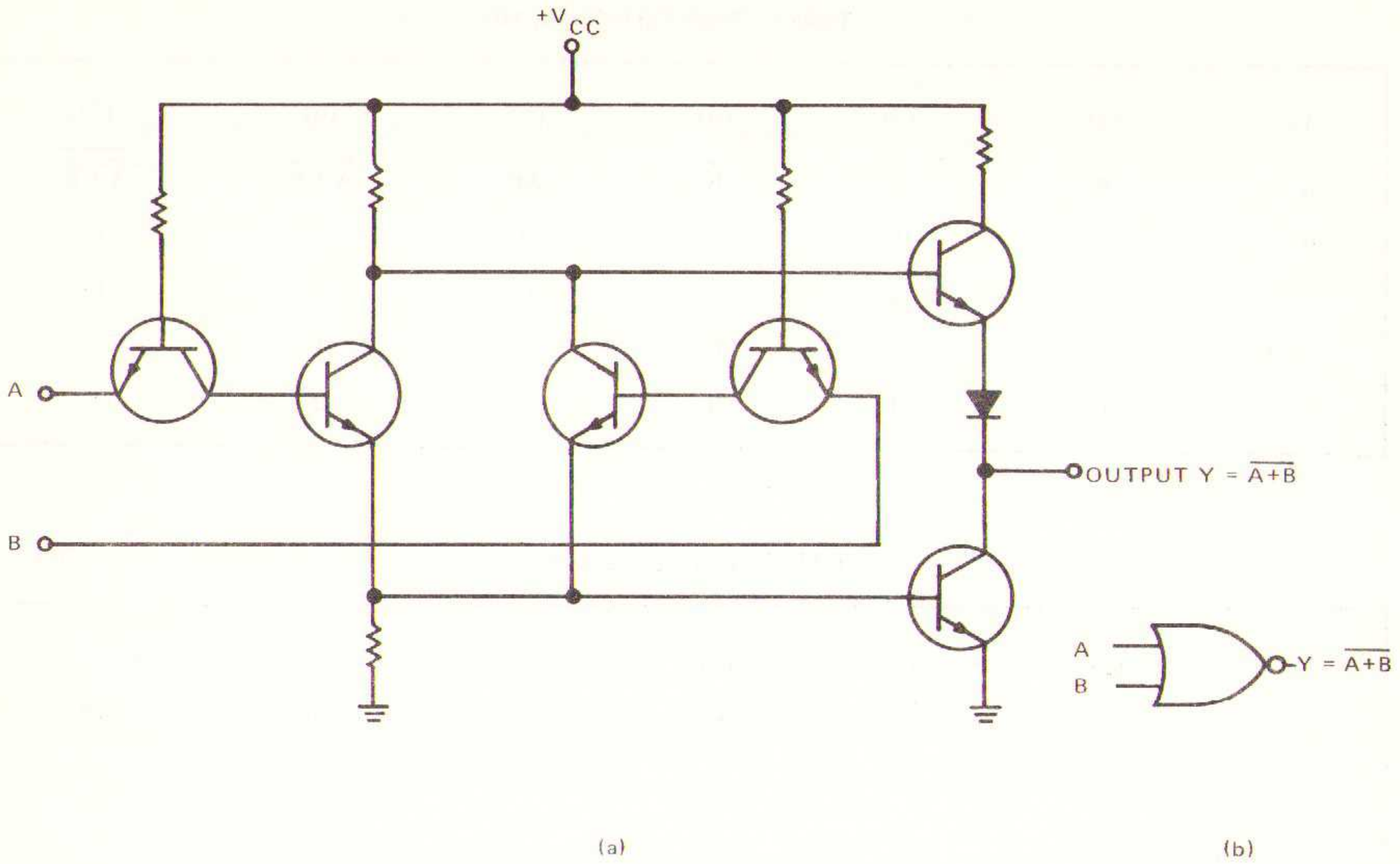


FIGURE 4. Circuit and Symbol for Series 54/74 NOR Gate

near ground potential. Hence, the circuit performs the NOR function. Figure 4(b) shows the logic diagram for this circuit.

Both the NAND and NOR gates become inverters when only one input signal is used. All input emitters of the NAND gate should be tied together if maximum switching speed is desired. Alternatively, the input signal may be applied to only one emitter of the NAND gate, with all other input emitters left open-circuited; this gives a slightly slower operating speed. Unused inputs of the NOR gate should be grounded or else connected to an active input for maximum switching speed.

Two circuits of the 54/74 series – the SN5450/7450 and the SN5453/7453 – perform the AND-OR-Invert function. Unused AND gates in these two circuits should have at least one input grounded.

LOGIC-CIRCUIT DESIGN

The following two identities of Boolean algebra are important for this analysis

$$AB = \overline{\bar{A} + \bar{B}} \tag{6}$$

$$A+B = \overline{\bar{A}\bar{B}} \tag{7}$$

The validity, or truth, of these expressions is proven by forming two truth tables: this is shown in Tables 1 and 2 for eqs. (6) and (7), respectively. A comparison of columns 5 and 7 in Table 1 shows that eq. (6) is true. The validity of eq. (7) is seen by comparing columns 5 and 7 of Table 2.

Eq. (6) shows that the AND function of two terms can be obtained by forming the NOR combination of the complement of each term. From eq. (7), the OR function of

Table 1. Truth Table for Eq. (6)

(1)	(2)	(3)	(4)	(5)	(6)	(7)
A	B	$\overline{A}$	$\overline{B}$	AB	$\overline{A} + \overline{B}$	$\overline{\overline{A} + \overline{B}}$
0	0	1	1	0	1	0
1	0	0	1	0	1	0
0	1	1	0	0	1	0
1	1	0	0	1	0	1

Table 2. Truth Table for Eq. (7)

(1)	(2)	(3)	(4)	(5)	(6)	(7)
A	B	$\overline{A}$	$\overline{B}$	A + B	$\overline{A}\,\overline{B}$	$\overline{\overline{A}\,\overline{B}}$
0	0	1	1	0	1	0
1	0	0	1	1	0	1
0	1	1	0	1	0	1
1	1	0	0	1	0	1

two terms is obtained by forming the NAND combination of the complement of each term. These two equations can be expanded to any number of terms; this permits NOR and NAND gates having n inputs to provide AND and OR functions, respectively, for up to n terms.

Logic expressions containing various combinations of AND and OR functions may be implemented by using combinations of gates. For instance, the function $\overline{AB+CD}$ is obtained with the two NAND gates of Figure 3. An inverter may be added at the output of this circuit to provide AB+CD. Another method for obtaining AB+CD is shown in Figure 5. NAND gates N_1 and N_2 provide $\overline{AB}$ and $\overline{CD}$, respectively. These two terms are combined in NAND gate N_3 to yield

$$\text{OUTPUT Y} = \overline{(\overline{AB})\,(\overline{CD})} \qquad (8)$$

Compare the above expression with the right side of eq. (7); this allows us to write

$$\text{OUTPUT Y} = AB + CD \qquad (9)$$

Circuit configurations for providing various logic functions are listed in Tables 3 through 6. The simple AND and OR

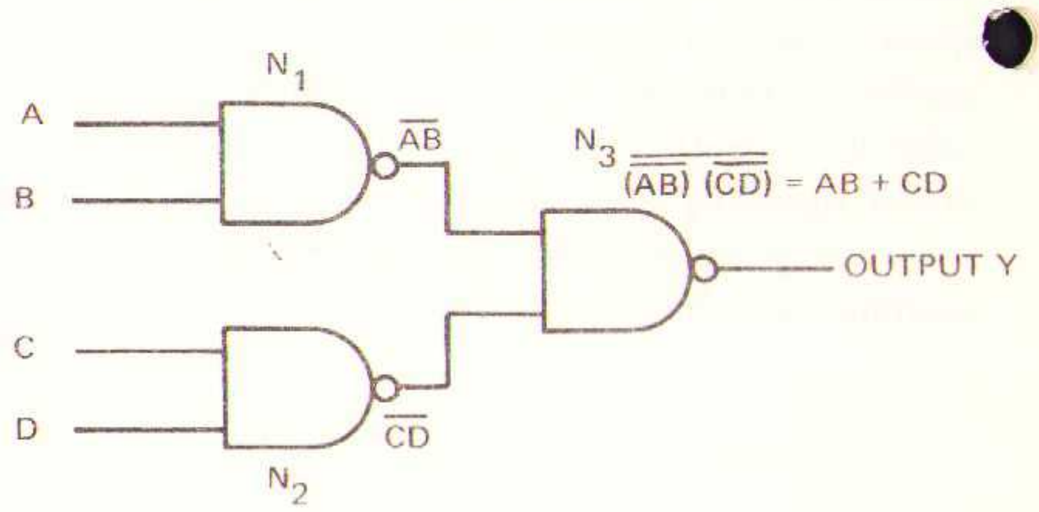


FIGURE 5. Three NAND Gates Performing AND-OR Function Y = AB + CD

Table 3. Logic-circuit Configuration for AND Functions

Logic Function	SN Type	No. of Circuits Used	No. of Packages	No. of Unused Circuits in Package	Figure	Inputs
AB	5400/7400	2	1	2	6	True
AB	5402/7402	1	1	3	7	Complement
AB	5401/7401*	2	1	2	8	Complement
AB	5450/7450**	1	1	1	9	Complement
ABC	5410/7410	2	1	1	10	True
ABCD	5420/7420	2	1	0	11	True
ABCD	5453/7453**	1	1	0	12	Complement
ABCDEFGH	5430/7430	1	1	0	13	True
	5400/7400	1	1	3		

*Five additional terms may be AND'ed by connecting the collectors of five additional SN5401/7401 gates.

**Four additional terms may be AND'ed by use of the SN5460/7460 expander element.

Table 4. Logic-circuit Configurations for OR Functions

Logic Function	SN Type	No. of Circuits Used	No. of Packages	No. of Unused Circuits in Package	Figure	Inputs
A + B	5402/7402	2	1	2	14	True
A + B	5401/7401*	2	1	2	15	True
	5400/7400	1	1	3		
A + B	5400/7400	1	1	3	16	Complement
A + B	5450/7450**	2	1	0	17	True
A + B + C	5410/7410	1	1	2	18	Complement
A+B+C+D	5453/7453**	1	1	0	19	True
	5400/7400	1	1	3		
A+B+C+D	5420/7420	1	1	1	20	Complement
A+B+C+D+E +F+G+H	5430/7430	1	1	0	21	Complement

*Five additional terms may be OR'ed by connecting the collectors of five additional SN5401/7401 gates.

**Four additional terms may be OR'ed by use of the SN5460/7460 expander element.

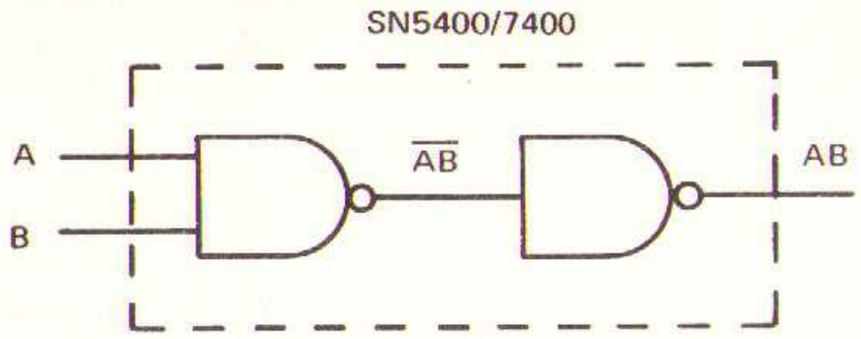


FIGURE 6. (See Table 3)

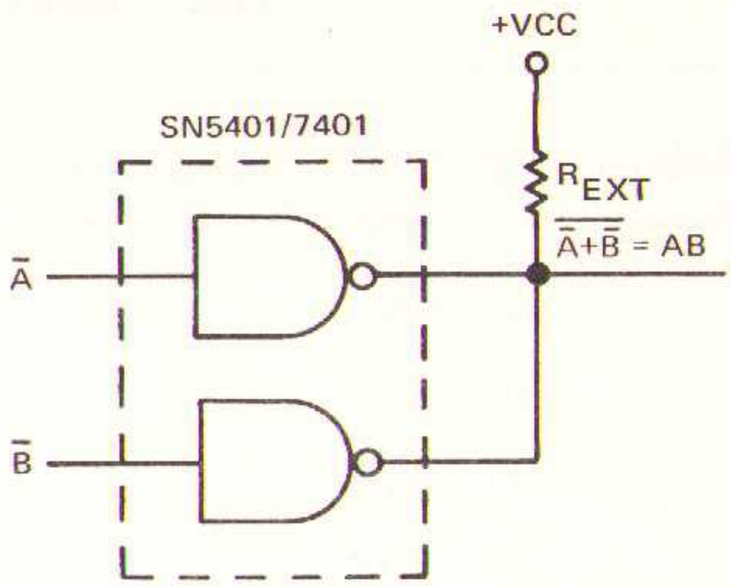


FIGURE 8. (See Table 3)

functions are given in Tables 3 and 4, respectively. Table 5 gives AND-OR functions, and Table 6 gives OR-AND functions. Each table lists the logic function, the SN type, the number of circuits used, the number of packages, the number of unused circuits in a package, the figure showing the particular logic-circuit configuration, and the type of inputs. Also of importance, but not shown, is the relative cost of each circuit configuration. This cost, which must be determined by the circuit designer, is based upon whether unused gates in a package will be applied elsewhere in the system. The availability of complemented inputs is another important consideration in selection of a logic-circuit configuration.

The circuit configurations in Figures 10, 11, 14, 17, 23, and 24 utilize the same gate element or elements for logic as well as for inversion at the output stage. Insofar as the particular logic implementation is concerned, this minimizes the number of packages, as all gates are on the same integrated chip. However, for systems containing several logic functions, it may be more economical to utilize a NAND or NOR gate within another package as the output inverter.

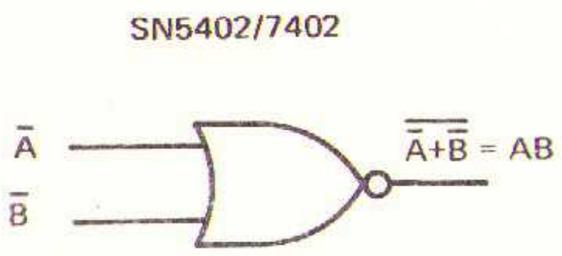


FIGURE 7. (See Table 3)

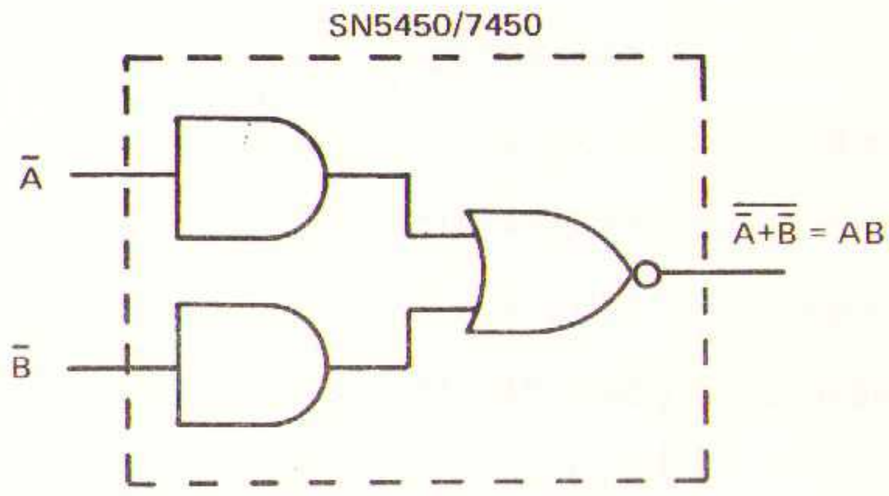


FIGURE 9. (See Table 3)

Table 5. Logic-circuit Configurations for AND-OR Functions

Logic Function	SN Type	No. of Circuits Used	No. of Packages	No. of Unused Circuits in Package	Figure	Inputs
AB + CD	5400/7400	3	1	1	22	True
AB + CD	5401/7401*	3	1	1	23	True
AB + CD	5450/7450**	2	1	0	24	True
AB+CD+EF	5453/7453**	1	1	0	25	True
+GH	5400/7400	1	1	3		
ABC + DEF	5410/7410	3	1	0	26	True
ABCD+EFGH	5420/7420	2	1	0	27	True
	5400/7400	1	1	3		
ABCDEFGH	5430/7430	2	2	0	28	True
+JKLMNPQR	5400/7400	1	1	3		

*Five additional 2-input AND terms may be OR'ed by connecting the collectors of five additional SN5401/7401 gates.

**Four additional 4-input AND terms may be OR'ed by use of the SN5460/7460 element.

Table 6. Logic-circuit Configurations for OR-AND Functions

Logic Function	SN Type	No. of Circuits Used	No. of Packages	No. of Unused Circuits in Package	Figure	Inputs
(A+B) (C+D)	5402/7402	3	1	1	29	True
(A+B) (C+D)	5401/7401*	2	1	2	30	Complement
(A+B) (C+D)	5450/7450**	1	1	1	31	Complement
(A+B) (C+D)	5453/7453**	1	1	0	32	Complement
(E+F) (G+H)						

*Five additional 2-input OR terms may be AND'ed by connecting the collectors of five other SN5401/7401 gates.

**Four additional 4-input OR terms may be AND'ed by use of the SN5460/7460 expander element.

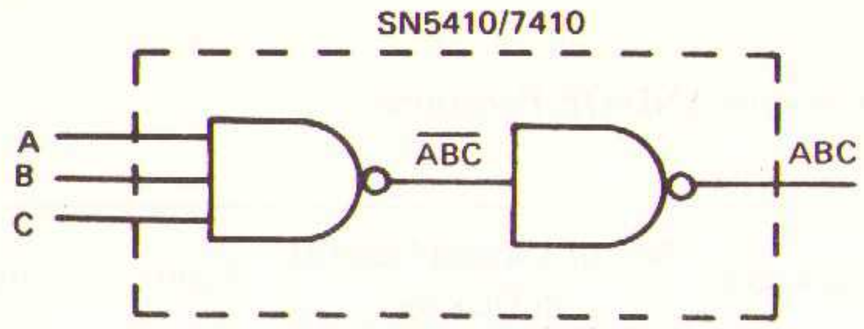


FIGURE 10. (See Table 3)

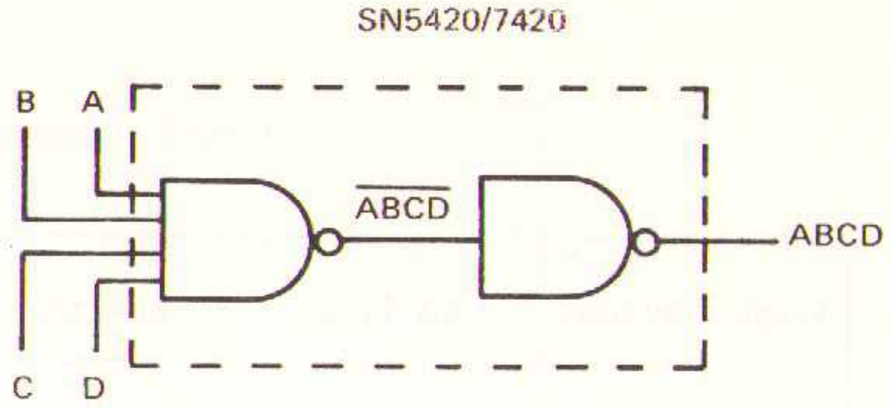


FIGURE 11. (See Table 3)

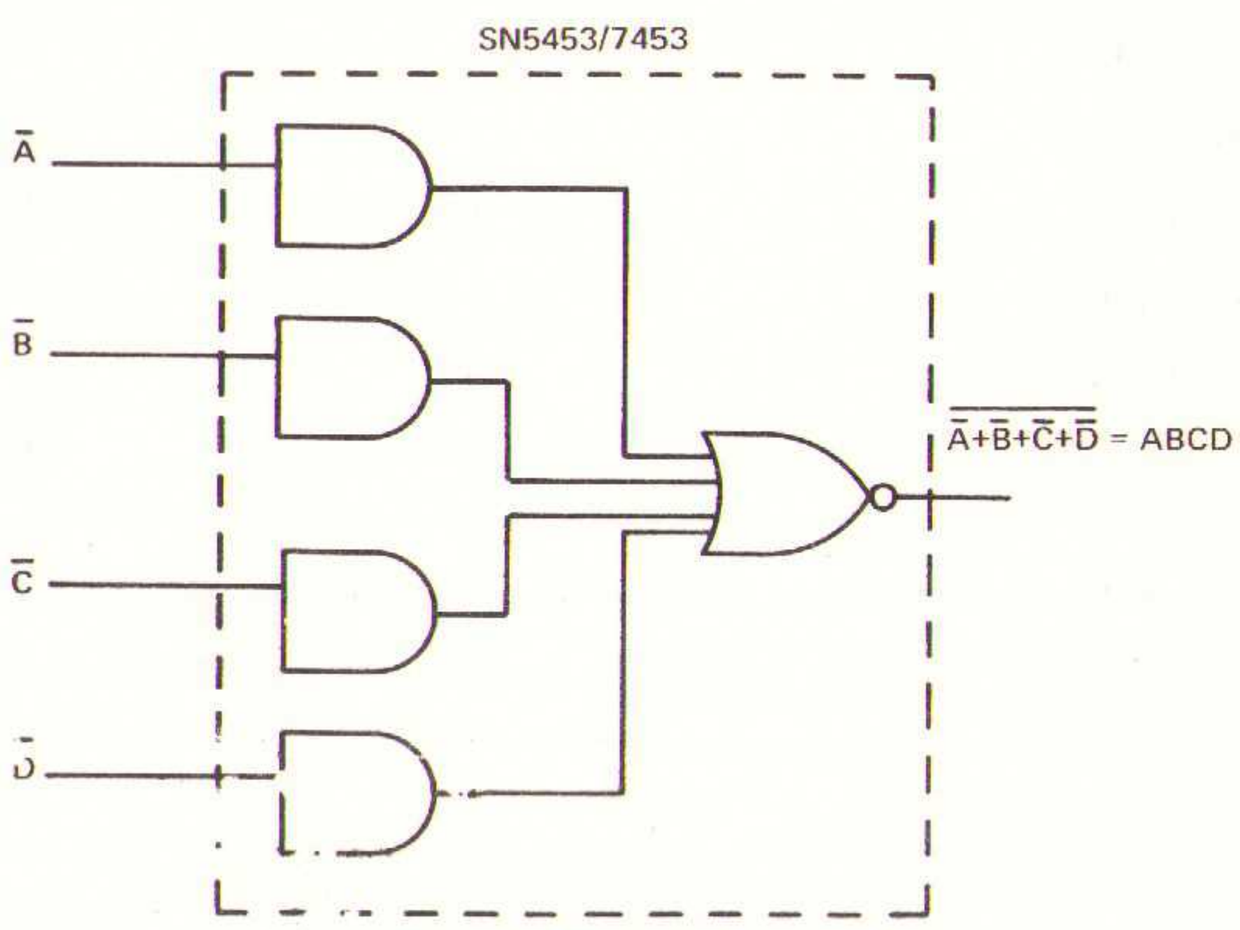


FIGURE 12. (See Table 3)

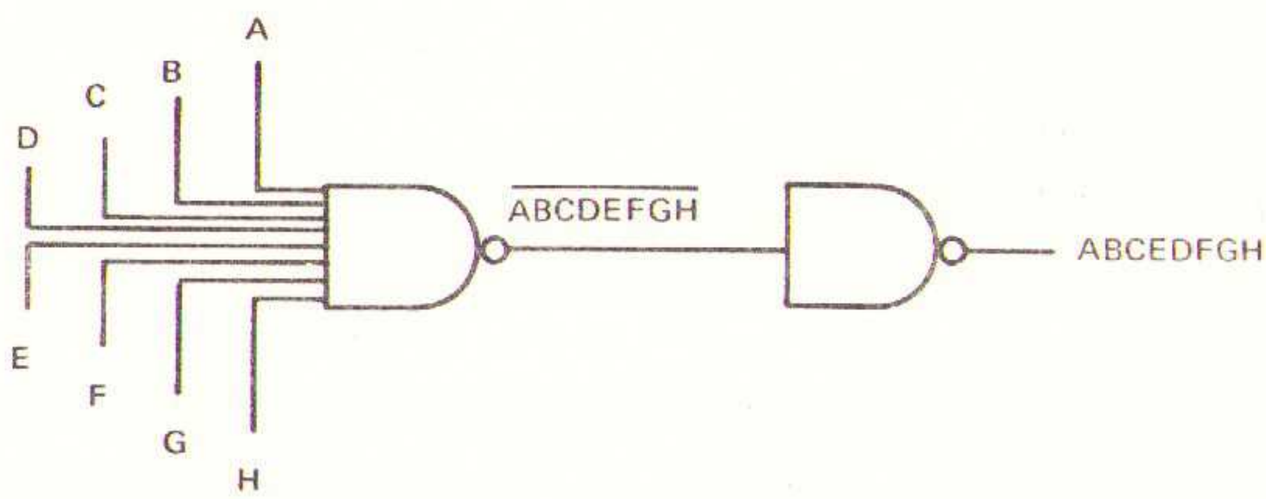


FIGURE 13. (See Table 3)

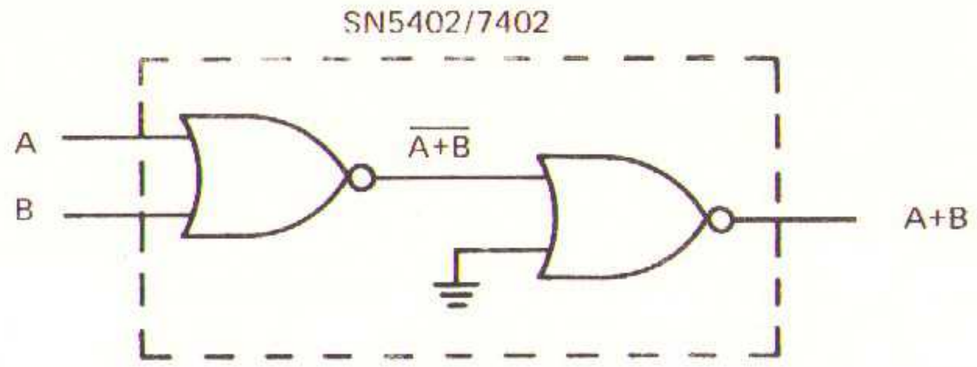


FIGURE 14. (See Table 4)

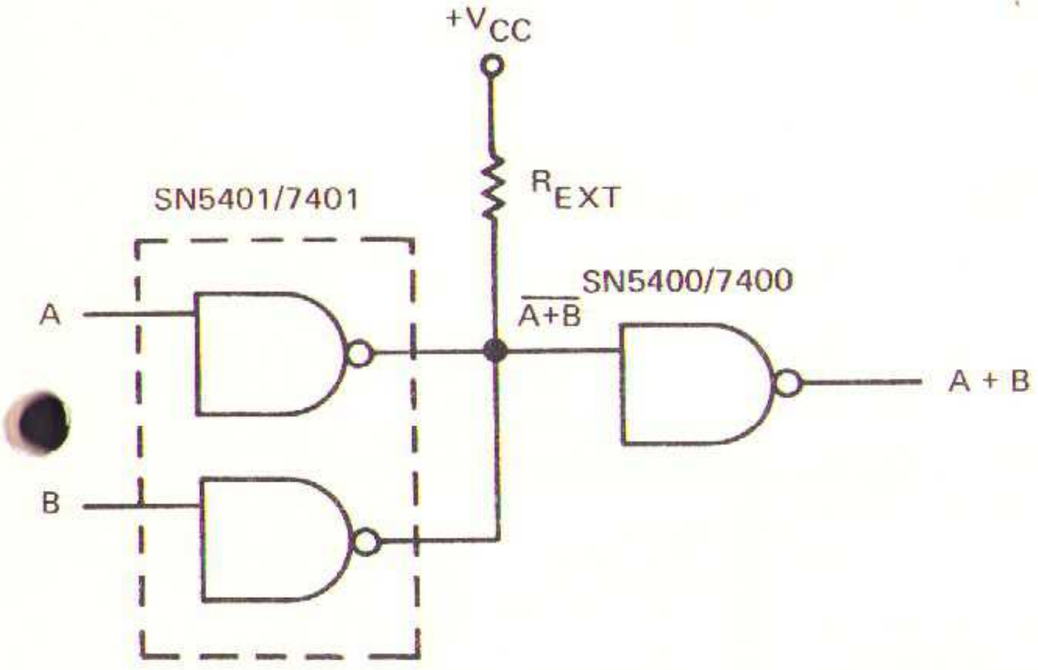


FIGURE 15. (See Table 4)

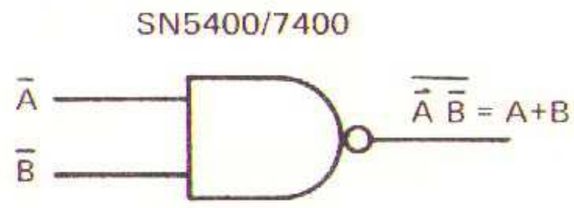
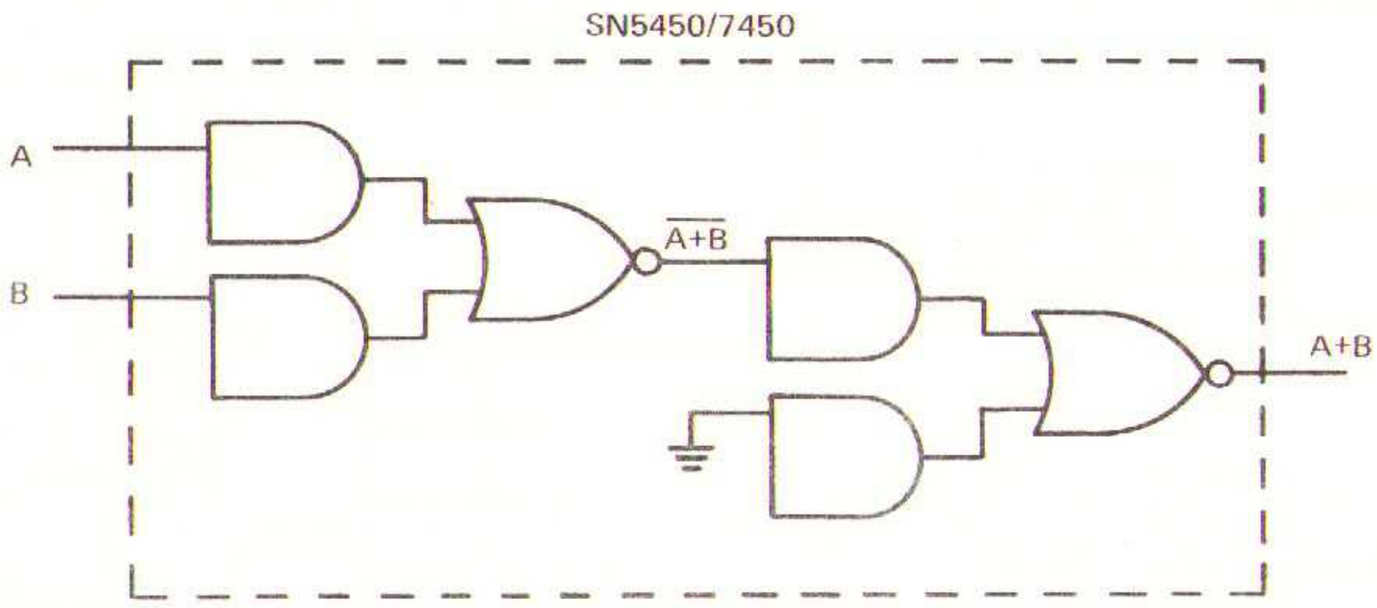


FIGURE 16. (See Table 4)



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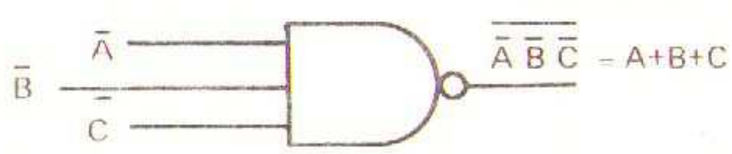


FIGURE 18. (See Table 4)

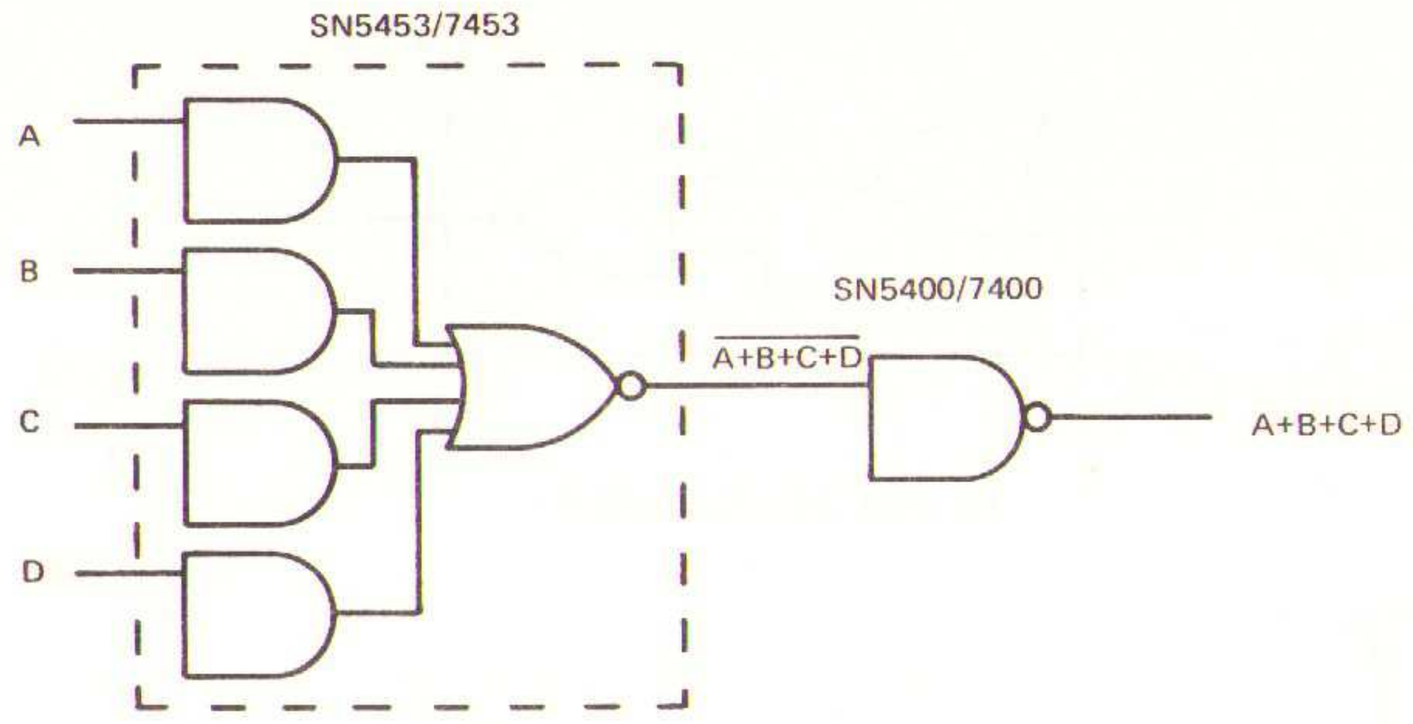


FIGURE 19. (See Table 4)

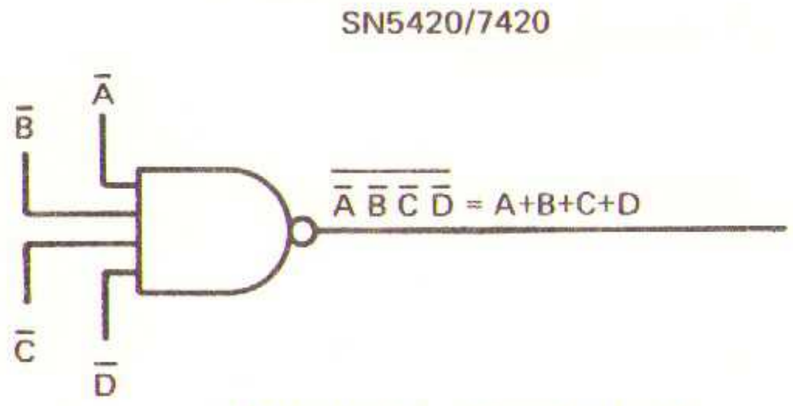


FIGURE 20. (See Table 4)

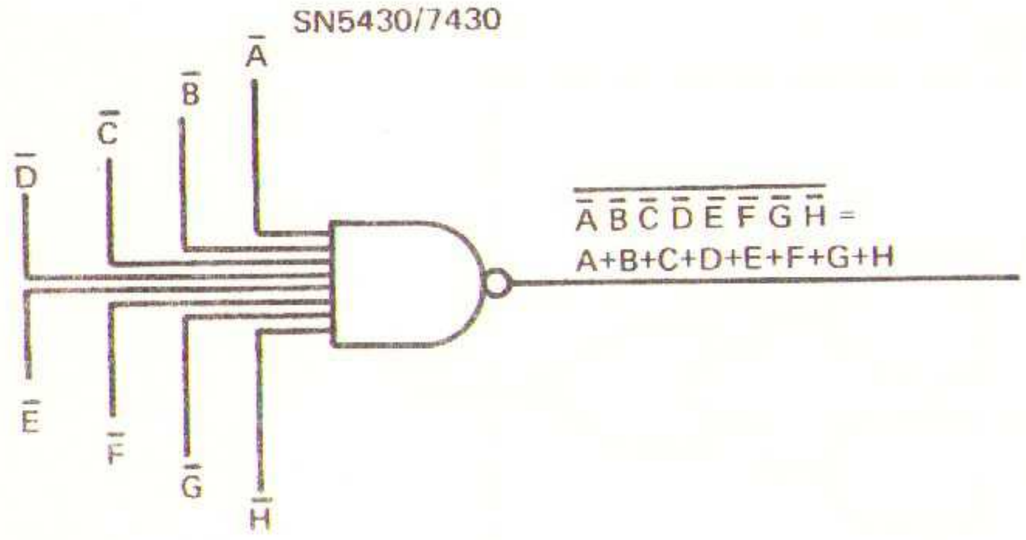


FIGURE 21. (See Table 4)

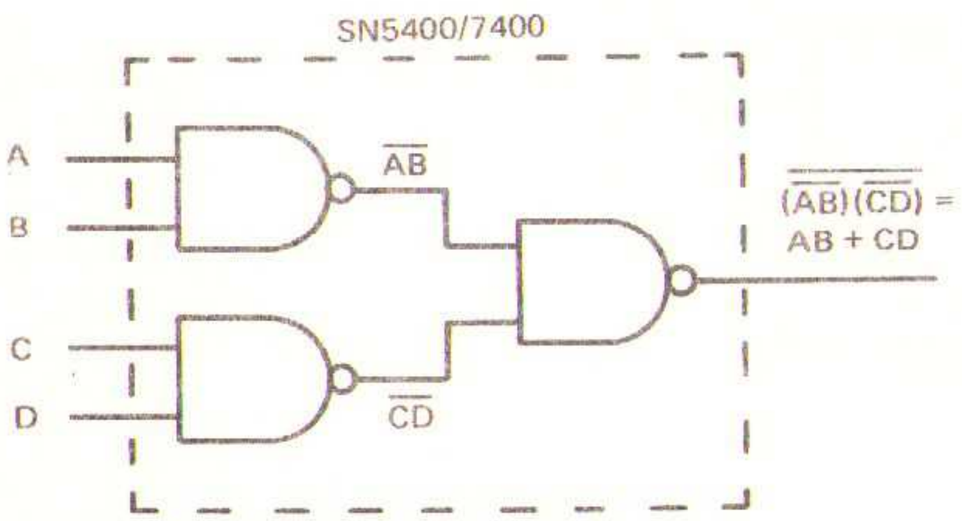


FIGURE 22. (See Table 5)

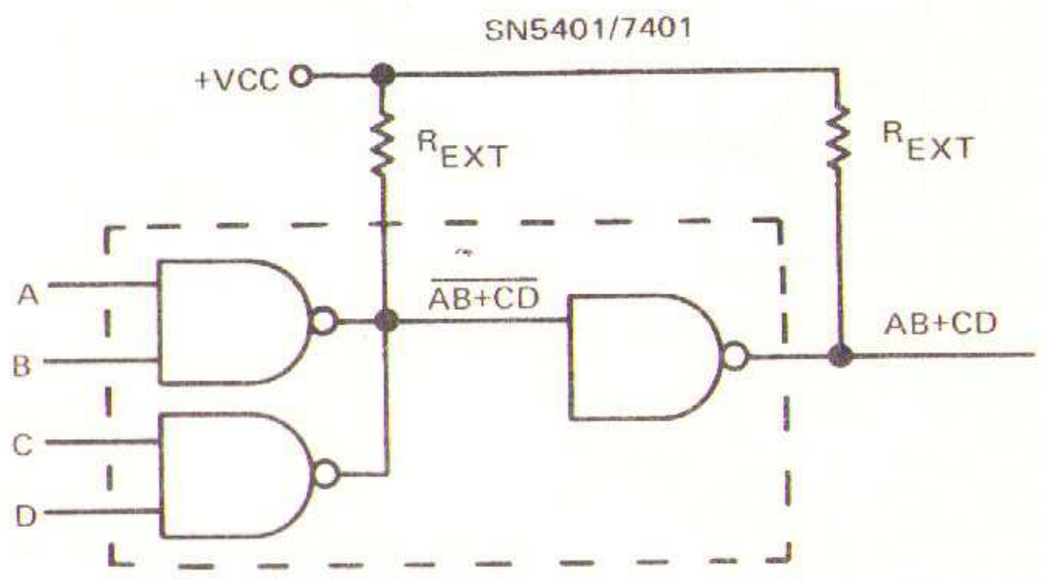
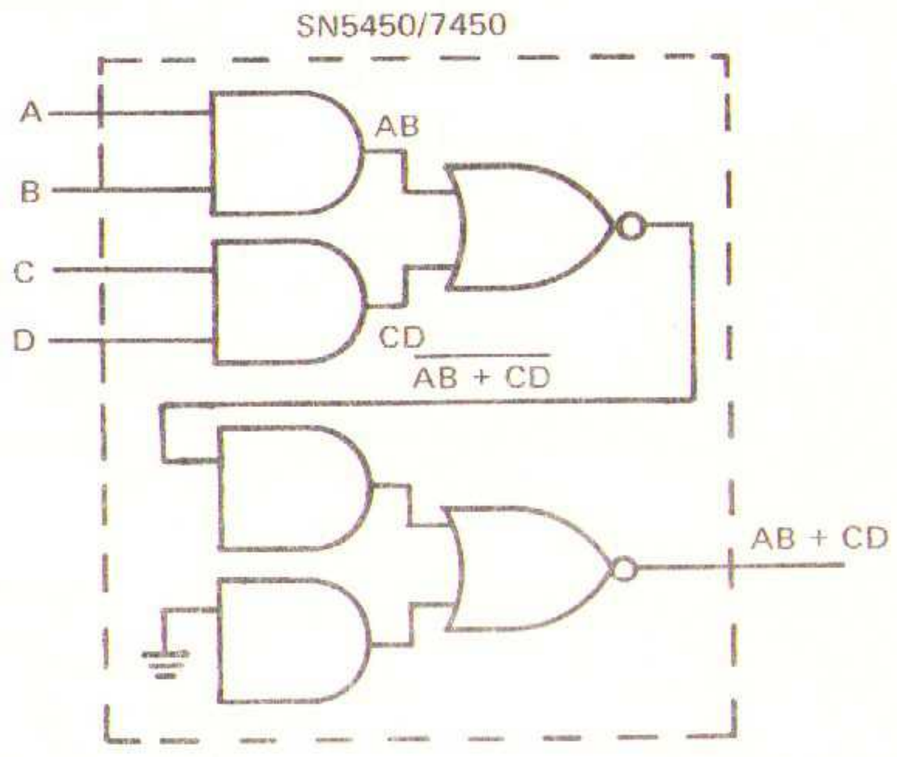


FIGURE 23. (See Table 5)



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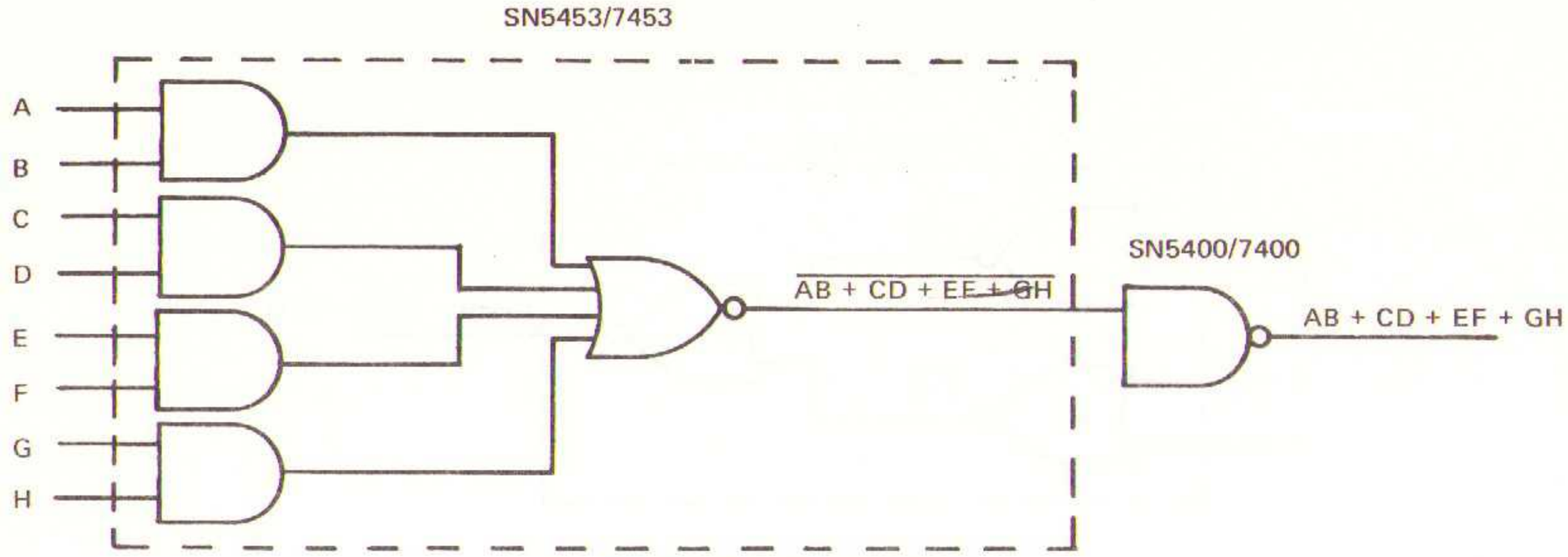


FIGURE 25. (See Table 5)

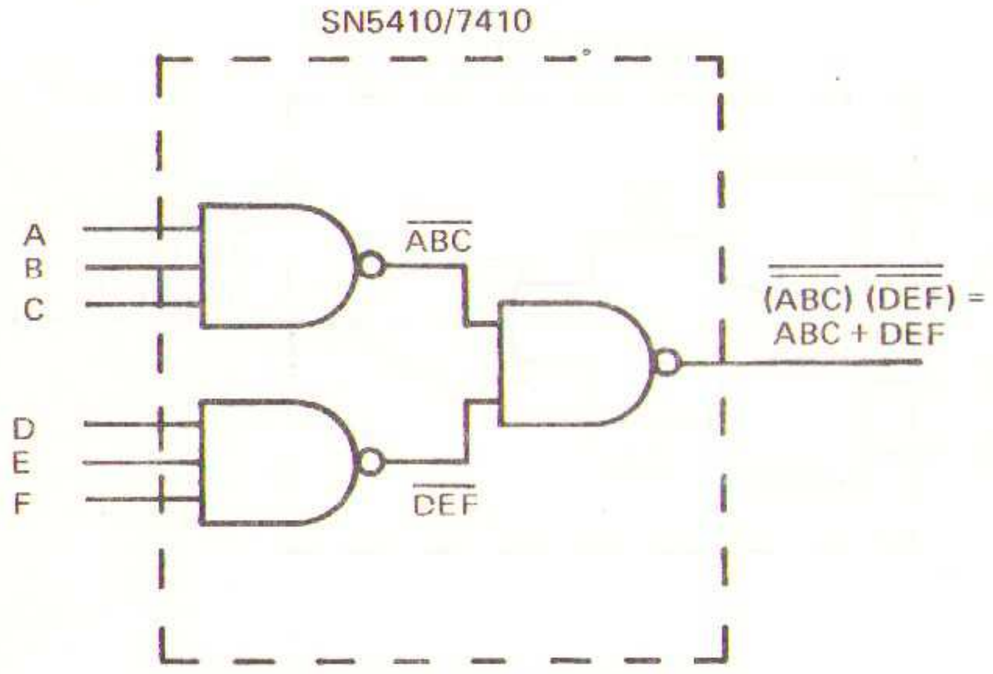


FIGURE 26. (See Table 5)

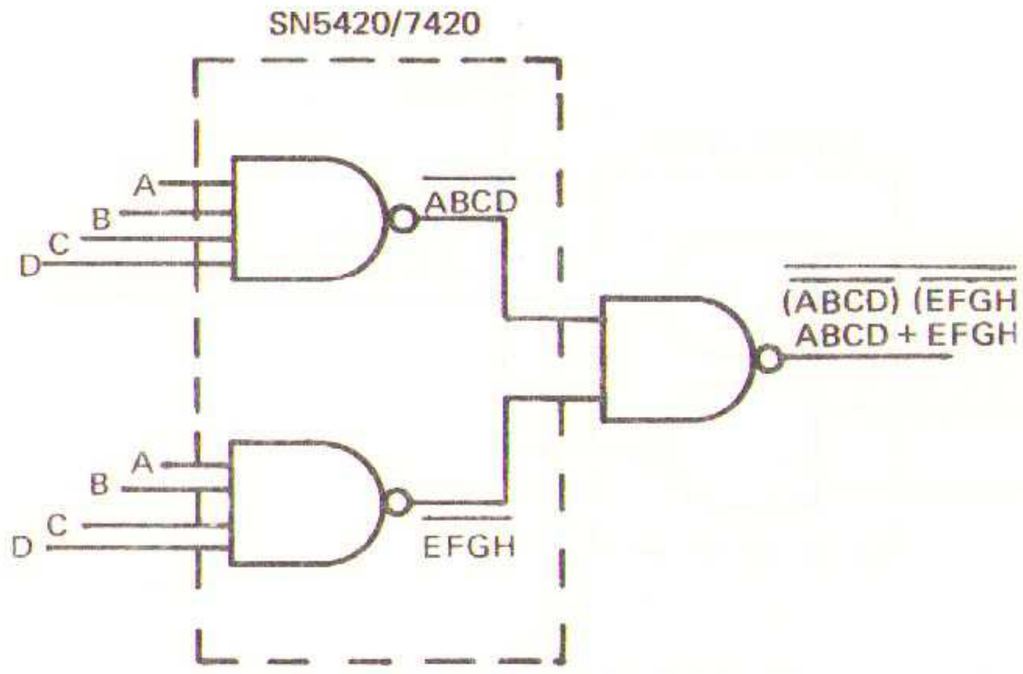


FIGURE 27. (See Table 5)

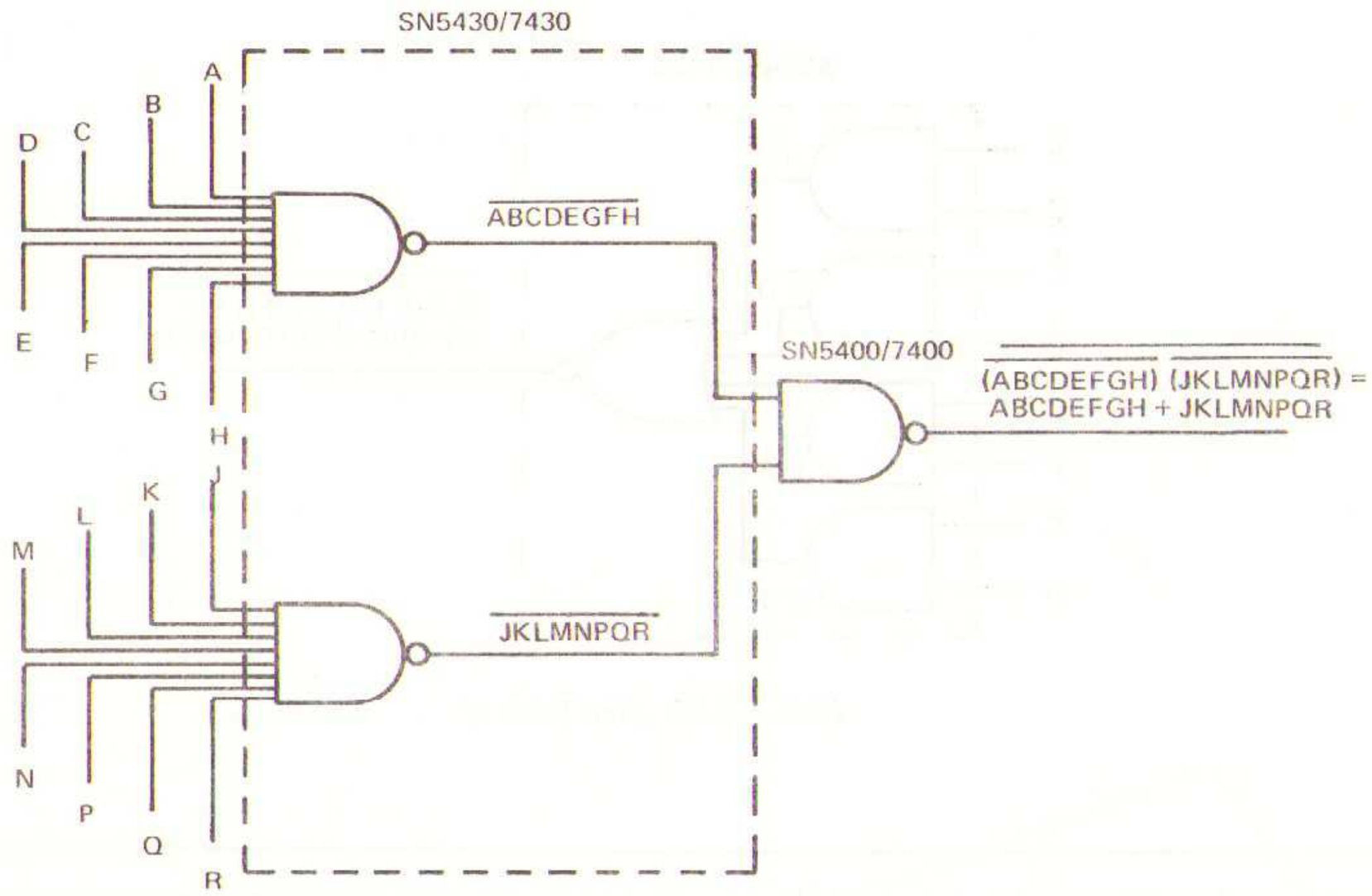


FIGURE 28. (See Table 5)

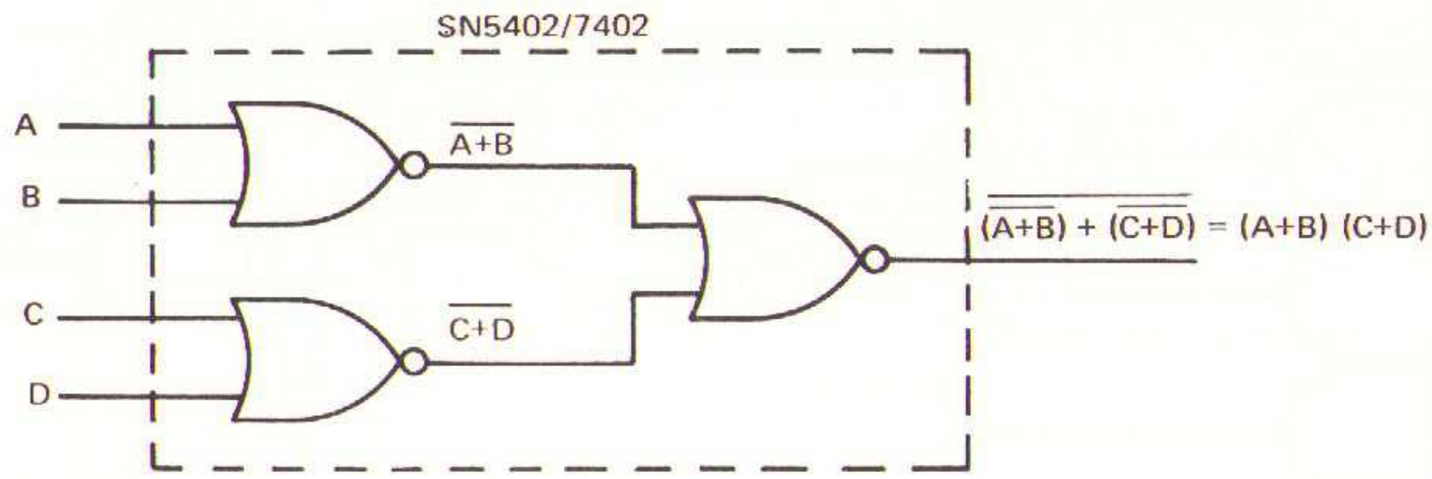


FIGURE 29. (See Table 6)

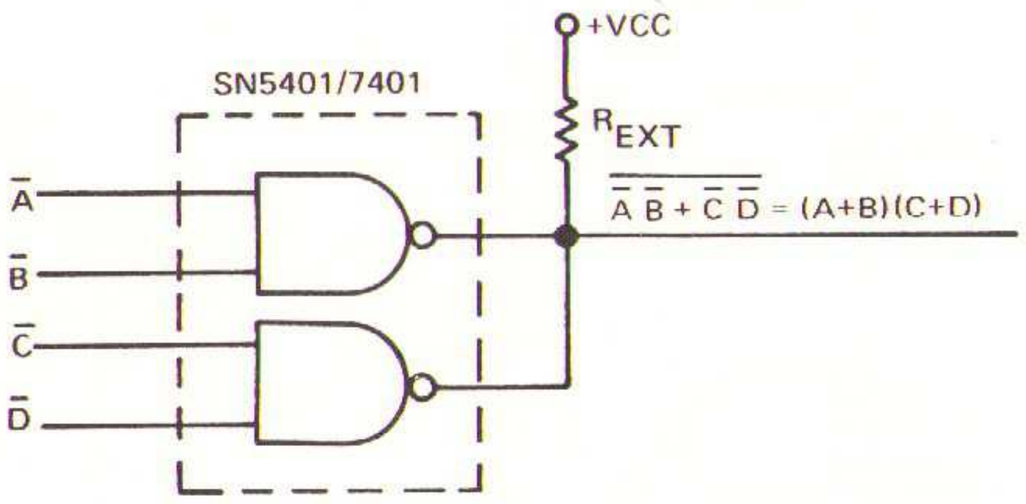


FIGURE 30. (See Table 6)

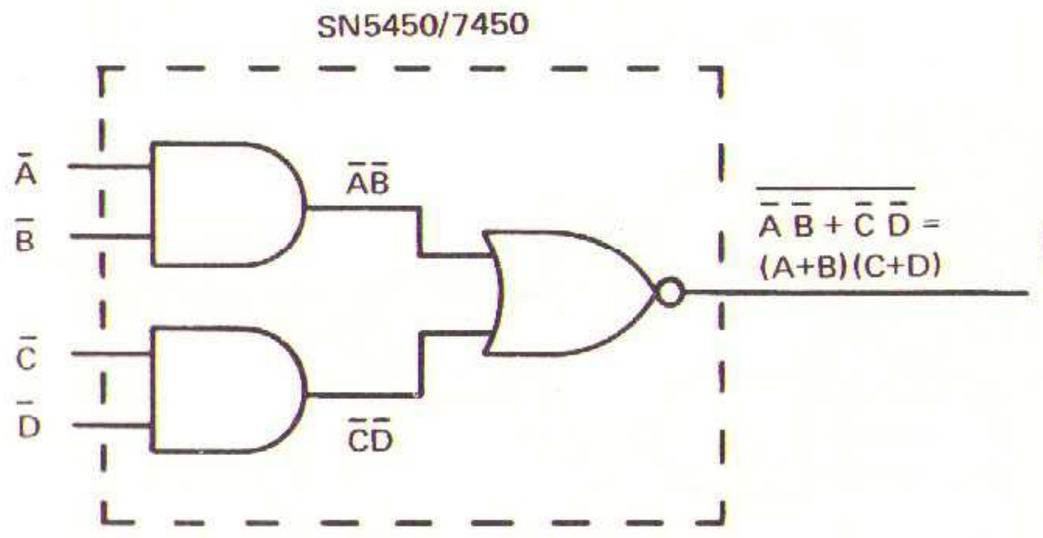


FIGURE 31. (See Table 6)

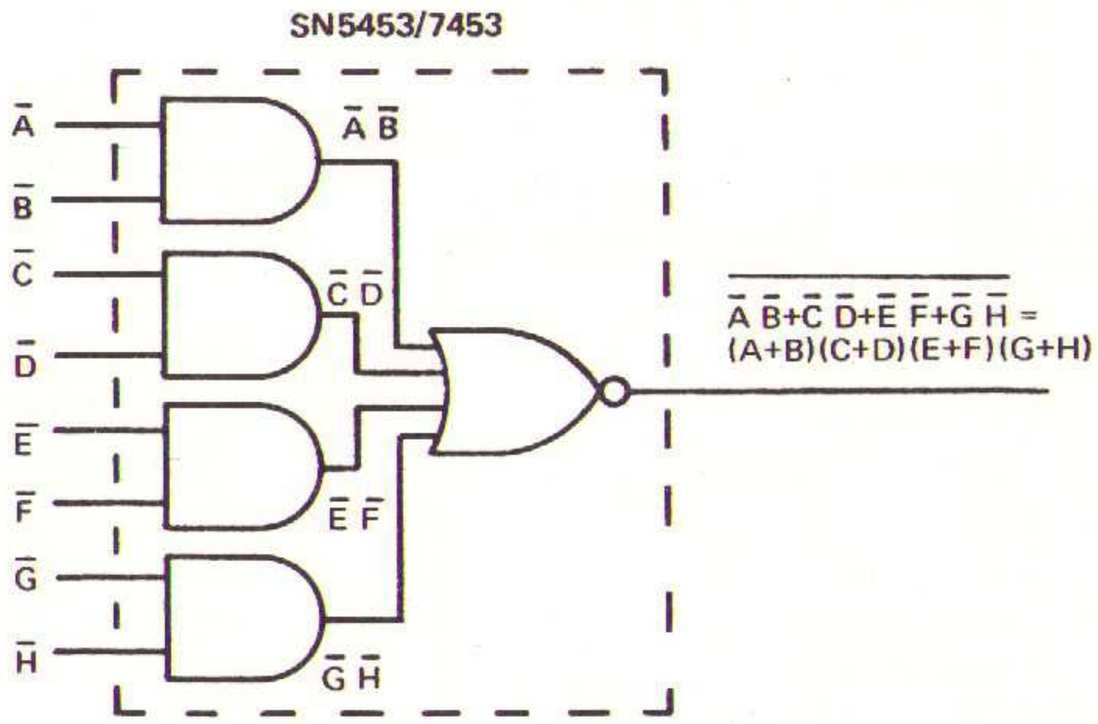


FIGURE 32. (See Table 6)

A A N T E K E N I N G E N

N O T E S

TTL INTEGRATED CIRCUITS: COUNTERS AND REGISTERS

Dietrich R. Erdmann

I. INTRODUCTION

The Series 74 TTL family of integrated circuits is the fastest, and most complete line of saturated, digital logic available today. In addition to the familiar basic TTL circuits, most gating and flip-flop functions are available in a high-speed and a low-power version. This combination of compatible circuits and the largest selection of MSI (medium scale integration) devices offers the design engineer considerable flexibility in the selection of speed versus power dissipation best suited for his system.

This application report consists of the functional analyses required to construct shift-or storage-registers and various types of counters using Texas Instruments Series 74 transistor-transistor logic (TTL) circuits. The information is primarily intended to assist in the utilization of complex Series 74 circuits; however, some examples require only the multifunction flip-flop or latch circuits. No detail, other than functional symbols, are provided for the gating functions unless special notations are required.

The devices specified throughout this report are basic Series 74 circuits in the familiar TTL configuration. These monolithic TTL circuits feature typical d-c noise margins of one volt, and full fan-out of 10 is available from all outputs. As some of the Series 74 MSI devices require 16 functional pins, circuits packaged in the molded dual-in-line package are used in the examples.

Registers and counters in the Series 54/74 TTL logic family now available are as follows:

SN7475 Quadruple Bistable Latch

SN7490 Decade Counter (Asynchronous)

SN7491 8-Bit Shift Register (Serial In/Serial Out)

SN7492 Divide-by-12 Counter

SN7493 4-Bit Binary Counter (Divide-by-16 Binary Counter)

SN7494 4-Bit Shift Register (Serial or Parallel In/Serial Out)

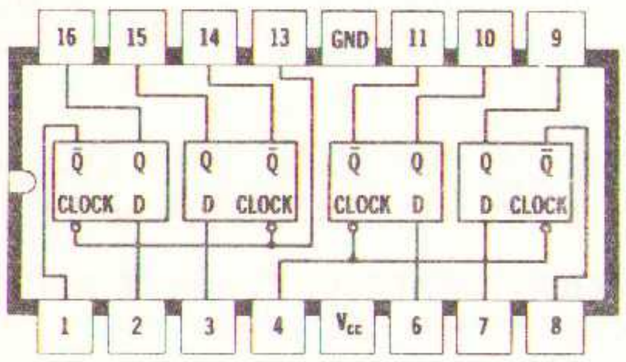
SN7495 4-Bit Shift-Right, Shift-Left Register (Serial or Parallel In/Serial and Parallel Out)

SN7496 5-Bit Shift Register (Serial or Parallel In/Serial and Parallel Out)

II. SERIES 74 SHIFT AND STORAGE REGISTER DESCRIPTIONS

A. QUADRUPLE BISTABLE LATCH SN7475

This quadruple, bistable latch is composed of four storage elements, each having complementary Q and $\overline{Q}$ outputs. See Figure 1. Information present at a data (D) input is transferred to the Q output if the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time this transition) occurred is retained at the Q output. Pin assignments were selected to coincide with the physical placement of logical functions of other Series 74 circuits which are likely to be used as inputs to, or outputs from, the SN7475.



PROPAGATION DELAY 30 NS
POWER DISSIPATION 160 MW

Figure 1. Quadruple Bistable Latch SN7475

This device is designed specifically for use as a temporary storage element between the SN7490 decade counter and the SN7441A binary-coded-decimal (BCD) to decimal decoder. See Figure 2. However, the simplicity of this particular storage function, and availability of complementary Q and $\overline{Q}$ outputs makes the SN7475 readily adaptable to other storage register applications.

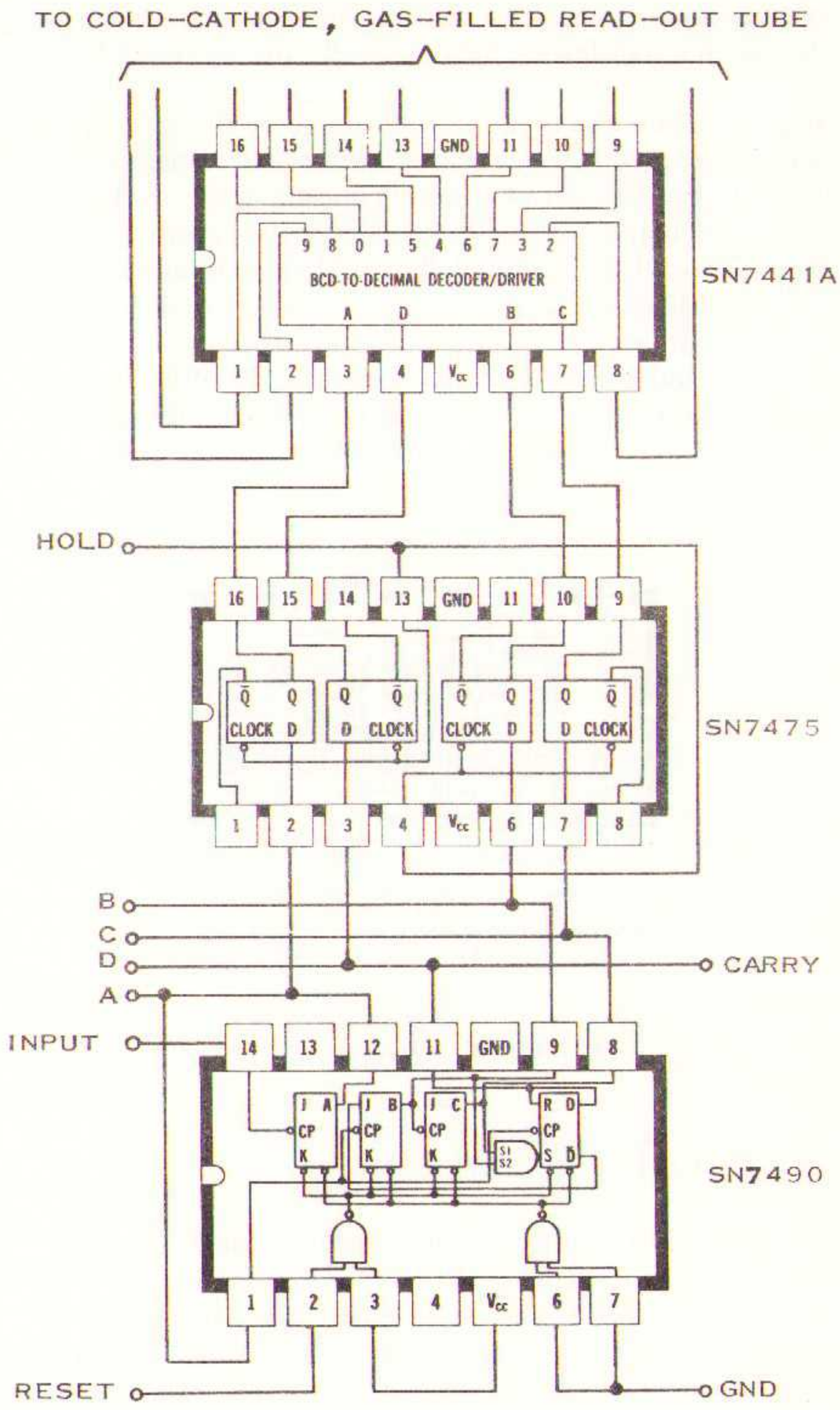


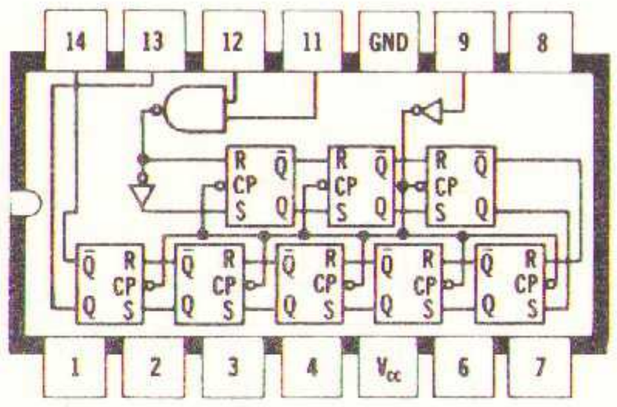
Figure 2. Storage and Readout of BCD Data From High-Speed Counter

B. 8-BIT SHIFT REGISTER SN7491A

This serial-in, serial-out, 8-bit shift register is composed of eight R-S master-slave flip-flops, input gating, and an inverting clock driver. See Figure 3. The register is capable of storing and transferring data at clock rates up to 18 MHz.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A,B, and CP) appears as only one TTL input load.

The clock pulse inverter/driver causes the SN7491A to shift information to the output on the positive edge of an input clock pulse.



PROPAGATION DELAY 25 NS
POWER DISSIPATION 175 MW

Figure 3. 8-Bit Shift Register SN7491A

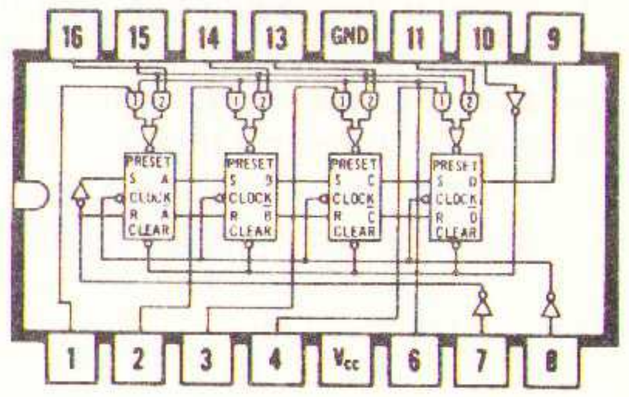
C. 4-BIT SHIFT REGISTER SN7494

This serial shift register is composed of four R-S master-Slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. See Figure 4. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register with parallel load capability or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops may be simultaneously set to the logical 0 state by applying a logical 1 voltage at the clear input. The register may be cleared independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state from either of two, gated, preset input sources. Preset inputs 1A through 1D are enabled during the time that a positive pulse is applied to preset 1, if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active, enabling the register to store a binary number or its complement.

Transfer of information to the output occurs on the positive edge of an input clock pulse or on the negative edge of a clock pulse. The proper information must appear at the R-S inputs of each flip-flop prior to the leading edge of the clock input waveform. The serial input provides this information to the first flip-flop while the outputs of each flip-flop provide information for the remaining R-S inputs.



PROPAGATION DELAY 25 NS
POWER DISSIPATION 175 MW

Figure 4. 4-Bit Shift Register SN7494

D. 4-BIT RIGHT-SHIFT/LEFT-SHIFT REGISTER SN7495

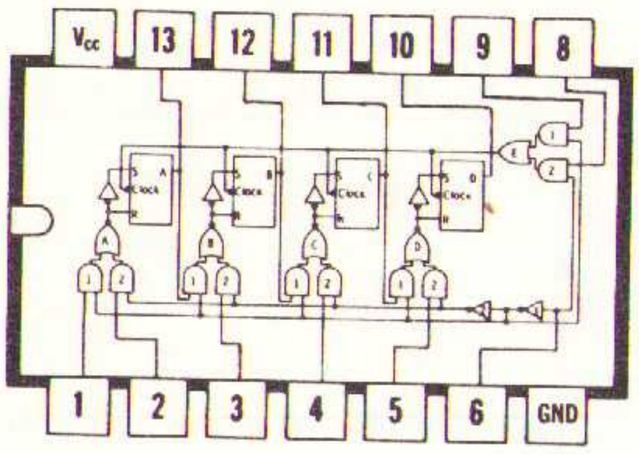
This parallel or serial shift register is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverter-drivers. See Figure 5. Internal interconnections of these functions provide a versatile register which will enter data serially or parallel dependent upon the logical input to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register by externally interconnecting each Q output to the parallel input of the preceeding bit.

When a logical 0 level is applied to the mode control input, the AND gates numbered "1" are enabled and the AND gates numbered "2" are inhibited. In this mode the Q output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the AND gates numbered "2".

When a logical 1 level is applied to the mode control input, the AND gates numbered "1" are inhibited (decoupling the Q outputs from the succeeding R-S inputs to prevent right-shift) and the AND gates numbered "2" are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register or, with external interconnection, shift-left operation.

Clocking for the shift register is accomplished through the AND-OR gate "E" which permits separate clock sources to be used for the right-shift and parallel-shift modes. If both

modes are to be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to the leading edge of the clock pulse.



PROPAGATION DELAY 25 NS
POWER DISSIPATION 250 MW

Figure 5. 4-Bit Right-Shift Left-Shift Register SN7495

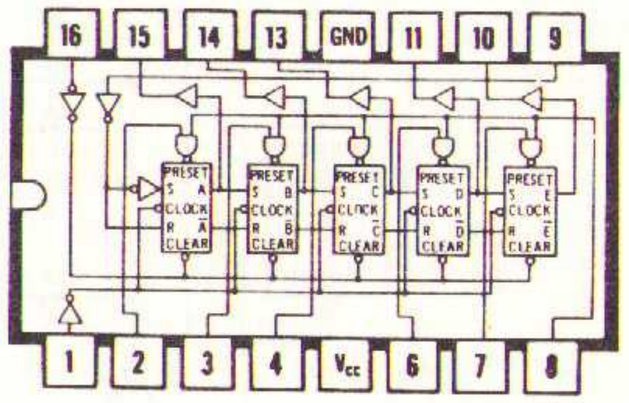
E. 5-BIT SHIFT REGISTER SN7496

This register consists of five R-S master-slave flip-flops connected as a shift register to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting all flip-flops simultaneously. Preset is also independent of the state of the clock input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of the first flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and at least one preset input of each flip-flop must be at a logical 0 when clocking occurs.



PROPAGATION DELAY 25 NS
POWER DISSIPATION 245 MW

Figure 6. 5-Bit Shift Register SN7496

III. LEFT/RIGHT SHIFT EXAMPLES

A. 6-BIT SHIFT-LEFT/SHIFT-RIGHT REGISTER WITH PARALLEL LOAD CAPABILITY

The 6-bit left- or right-shift register illustrated in Figure 7 demonstrates how a versatile serial-in or parallel-in register may be constructed using SN7474 flip-flops.

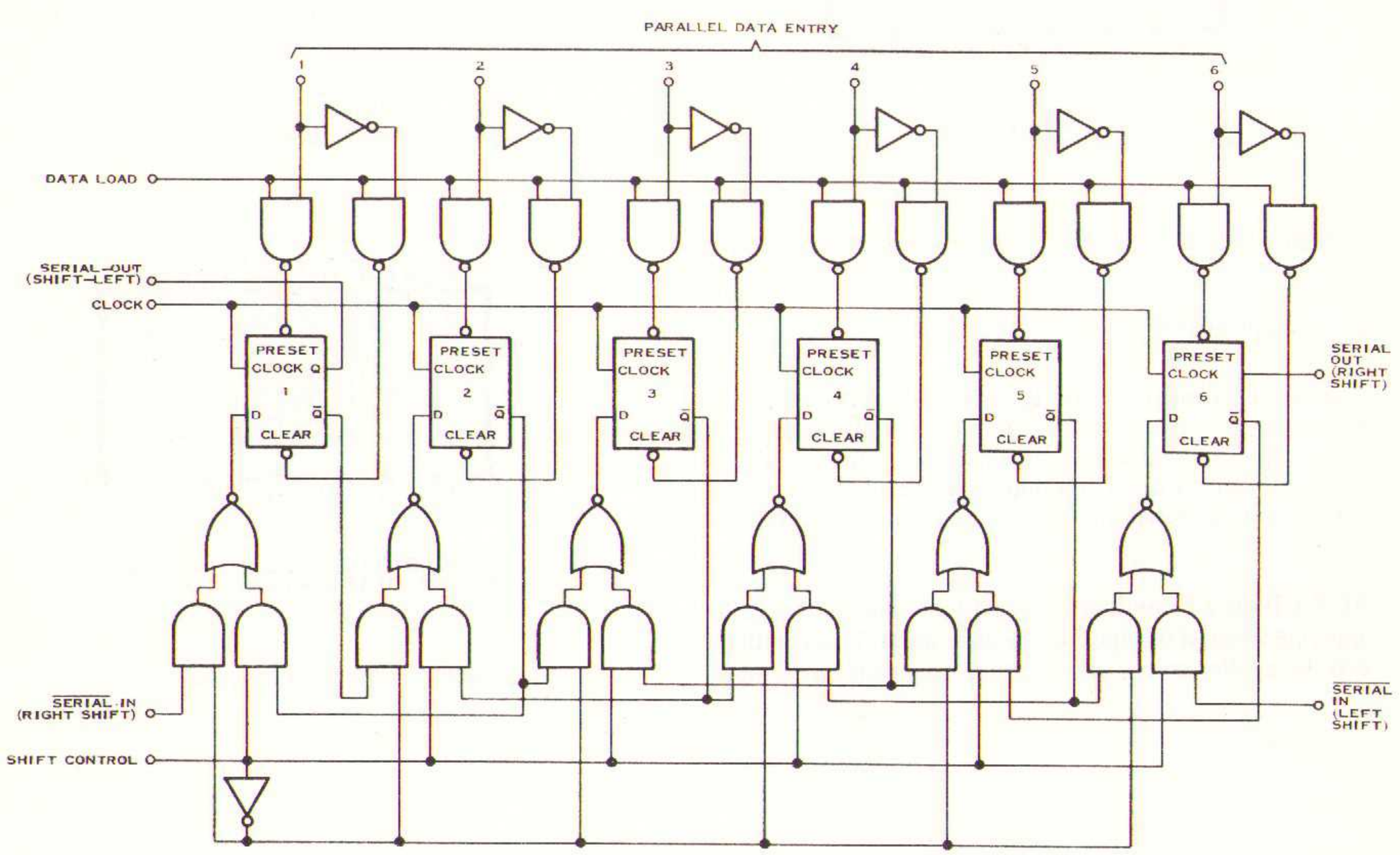


Figure 7. 6-Bit Left- or Right-Shift Register Using SN7474's

B. 8-BIT PARALLEL STORAGE REGISTER USING SN7495'S

The 8-bit parallel-entry, shift-left/shift-right register illustrated in Figure 8 utilizes two SN7495 shift registers. The SN7495 is particularly well suited for this application because it uses two clock lines. A continuous system clock may be applied to clock 2. The parallel data can be clocked in with mode control high. See Figure 8. Connecting Q_{II} and D_S (direct or gated) stores or circulates the data in the register. This holds for any number of cascaded SN7495's.

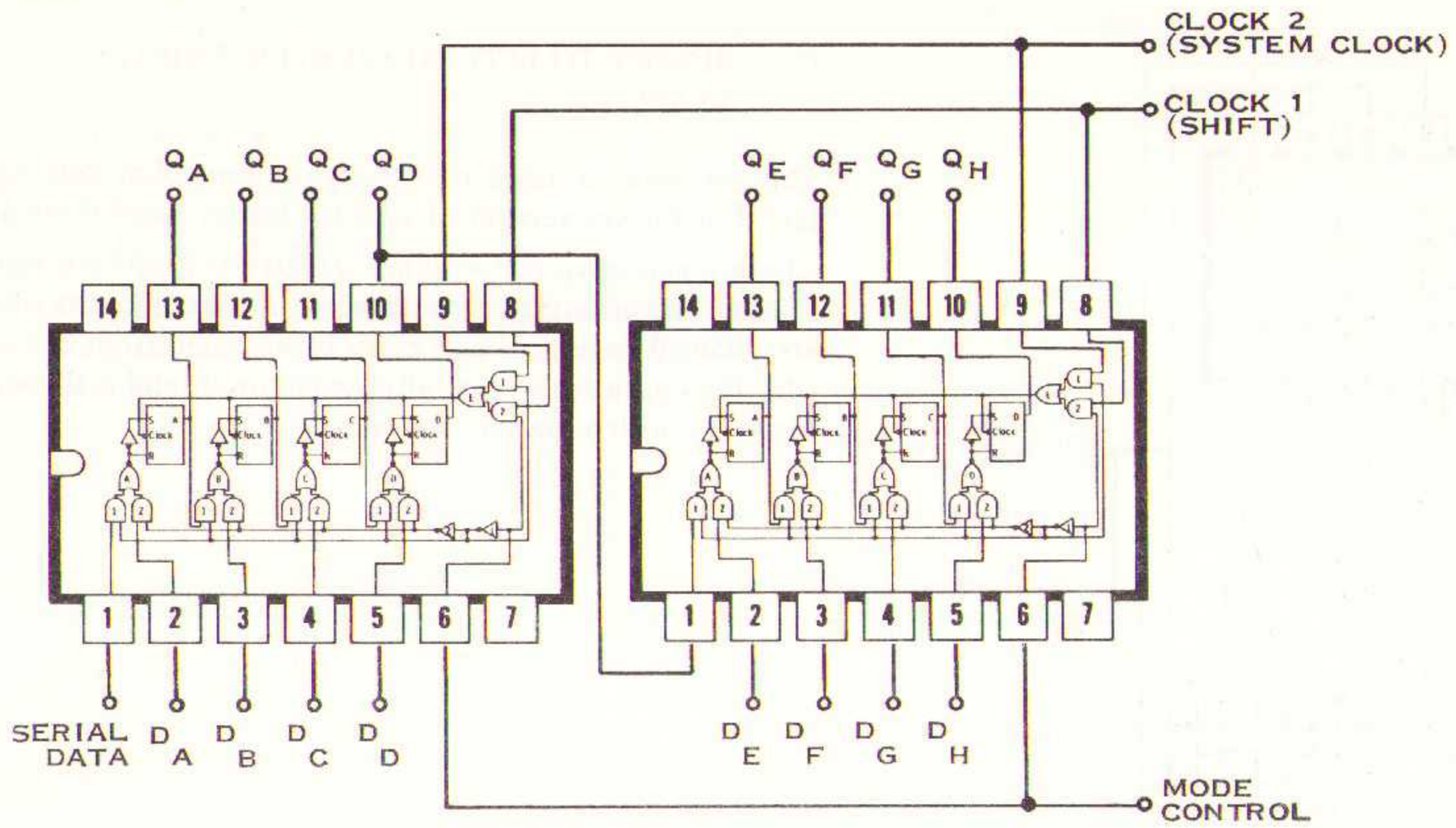


Figure 8. 8-Bit Parallel Storage Register Using SN7495's

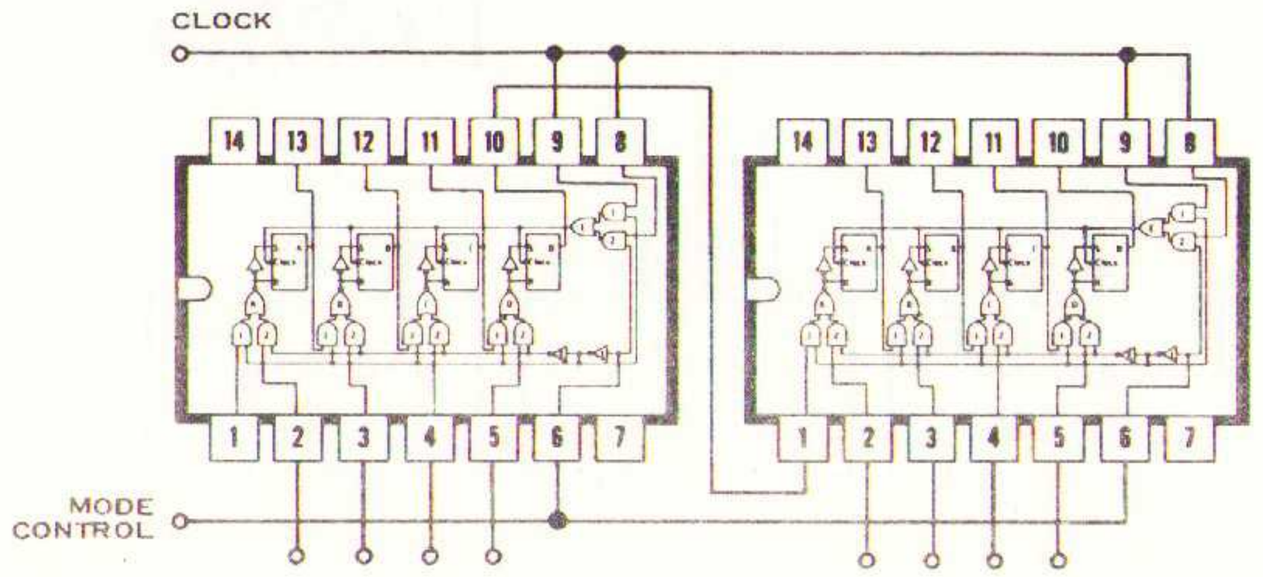
C. 8-BIT SHIFT-LEFT/SHIFT-RIGHT REGISTER USING SN7495'S

For left shift and parallel entry applications, the SN7495 may be used in two configurations.

1. When a binary word is defined with the bit to the right being the least significant bit (LSB), then if the LSB of the binary word to be stored and shifted is applied to the most significant bit position (MSB) of the SN7495 (right-most flip-flop Figure 9) and this word is shifted right, in effect a left shift is achieved.

   It can be seen that the effect of both operations is the same — left shift.

2. The outputs may be gated to the inputs for parallel entry and left shift. See Figure 10.



BINARY WORD	0	1	1	1		0	1	0	0
SHIFT LEFT	1	1	1	0		1	0	0	0
APPLY BINARY WORD IN INVERTED SEQ.	0	0	1	0		1	1	1	0
SHIFT RIGHT	0	0	0	1		0	1	1	1

Figure 9. 8-Bit Parallel-Entry, Left-Shift Register Using SN7495's

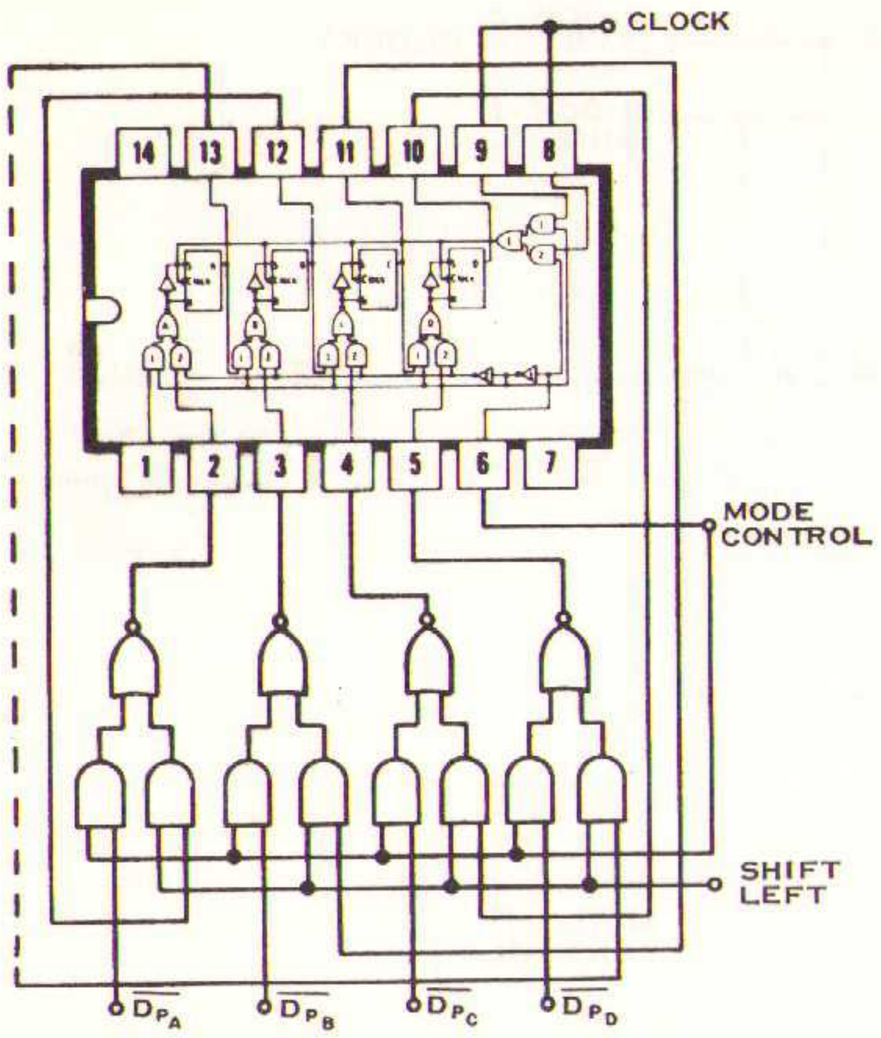


Figure 10. 4-Bit Parallel-Entry, Left-Shift Register Using SN7495

D. BINARY-TO-BCD CONVERTER USING SN7495's

This converter is based on the logical control of shift registers. For the conversion of an 8-bit binary word three decades are necessary ($2^8 = 256 = 2 \bullet 10^2 + 5 \bullet 10^1 + 6 \bullet 10^0$). The register outputs of each decade control the inputs which are disabled except when a carry is generated from this decade. The converter works fully synchronous and is shown in Figure 11 with a master clear input.

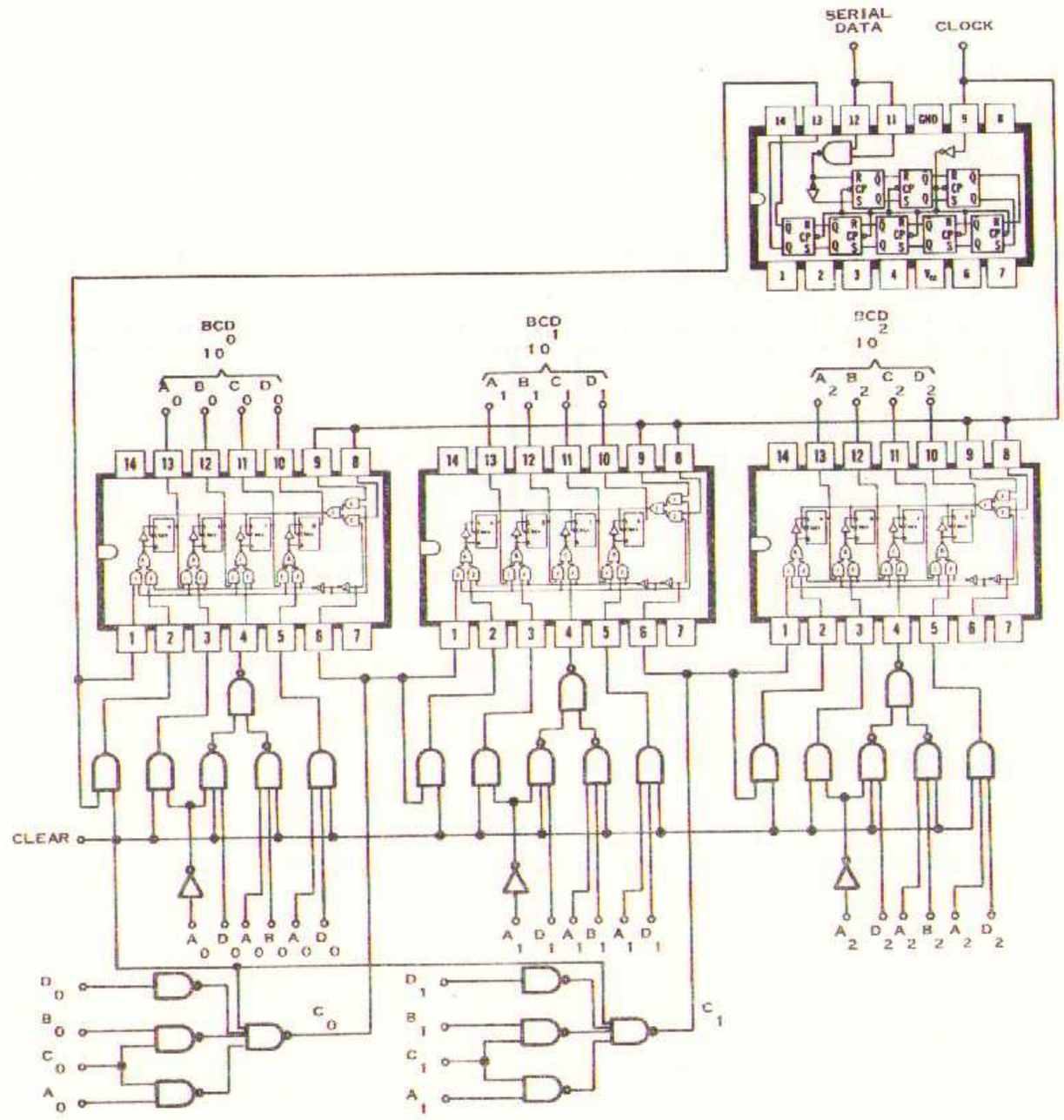


Figure 11. Binary-to-BCD Converter Using SN7495's

E. BCD-TO-BINARY CONVERTER USING SN7474'S

A Serial/Parallel BCD-to-Serial-Binary Converter using the SN7483 4-bit adder to make the required corrections is shown in Figure 11A. The flip-flops used are SN7474. Parallel entry is achieved with the asynchronous preset and clear inputs.

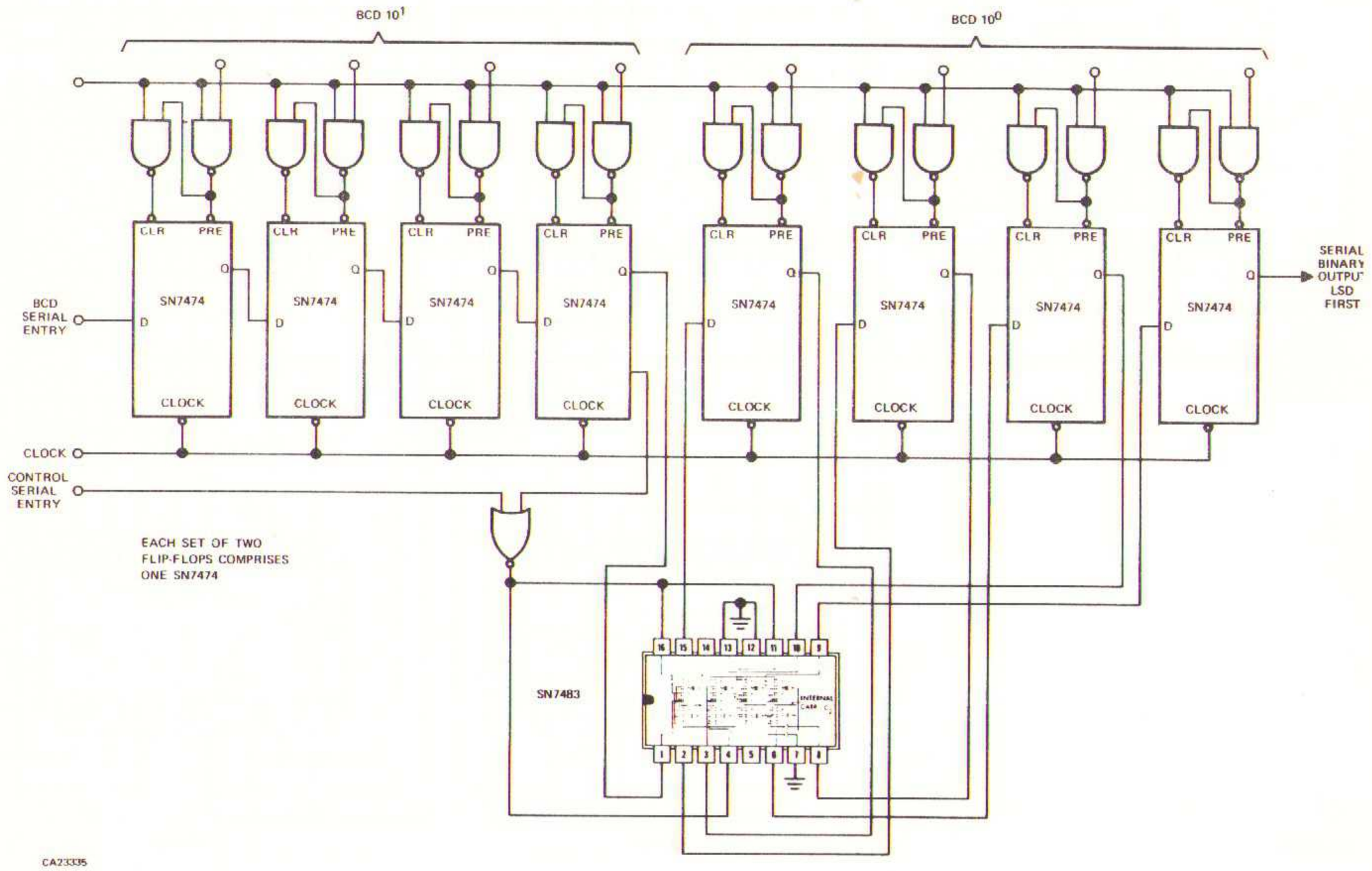


Figure 11A. BCD-To-Binary Converter Using SN7474's

Het is logisch, dat mensen, die logische schakelingen ontwikkelen, gebruik maken van TTL logische IC's.

F. SERIAL-BCD-TO-SERIAL BINARY CONVERTER USING SN7495'S

In Figure 11B, another version of a code converter (BCD-to-Binary) uses only two packages per decade: one SN7495 and one SN7483.

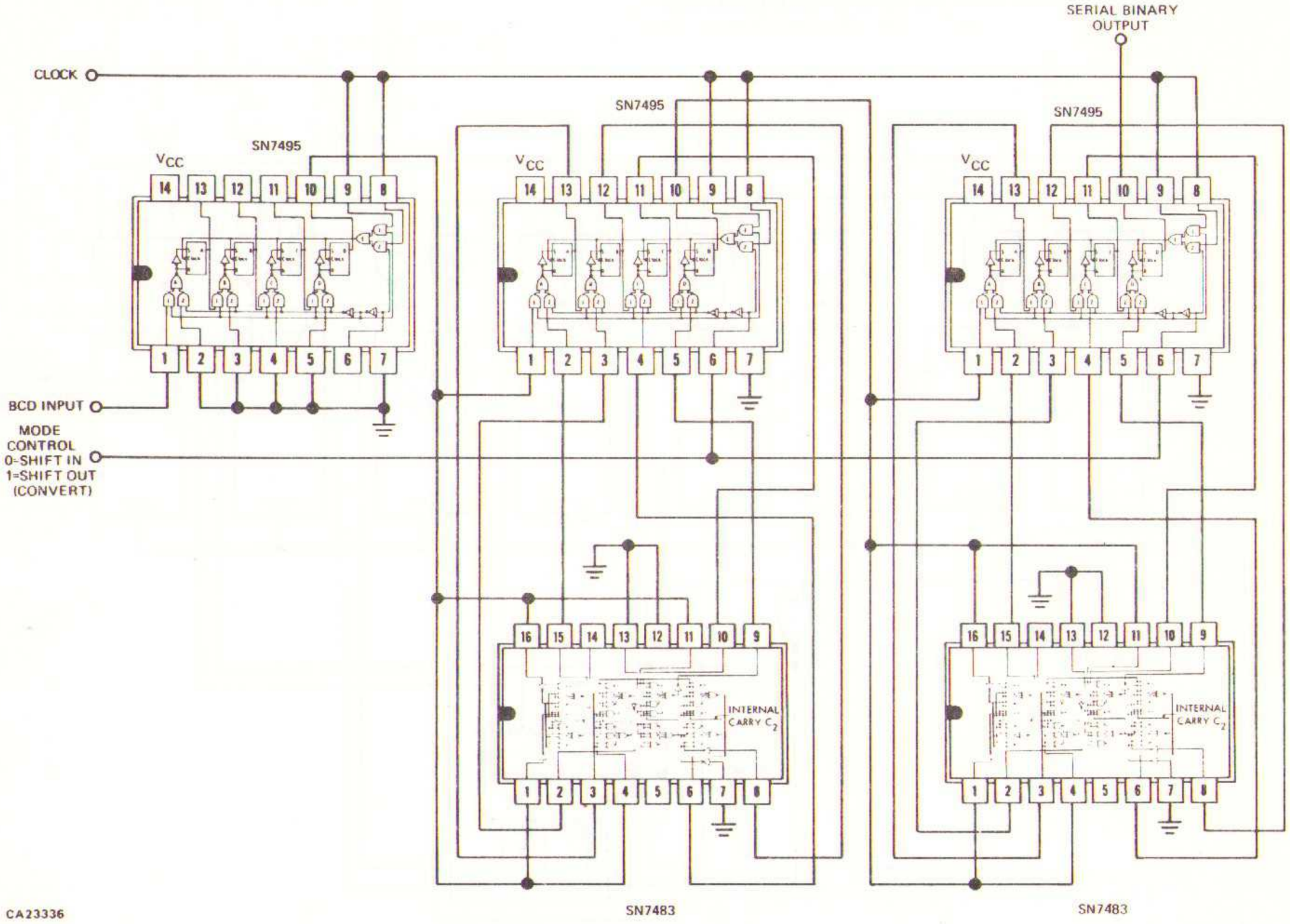


Figure 11B. Serial-BCD-To-Serial-Binary Converter (Three Decades) Using SN7495's

Wees niet van gisteren, gebruik vandaag TTL.

G. FOUR-BIT SERIAL SHIFT REGISTER USING SN7475'S

Although the SN7475 is a package with 4 bistable latches, data can be locked out by operating two latches in series as a master-slave flip-flop with a clock-inverter. A 4-bit shift register built with the SN7475 is shown in Figure 11C.

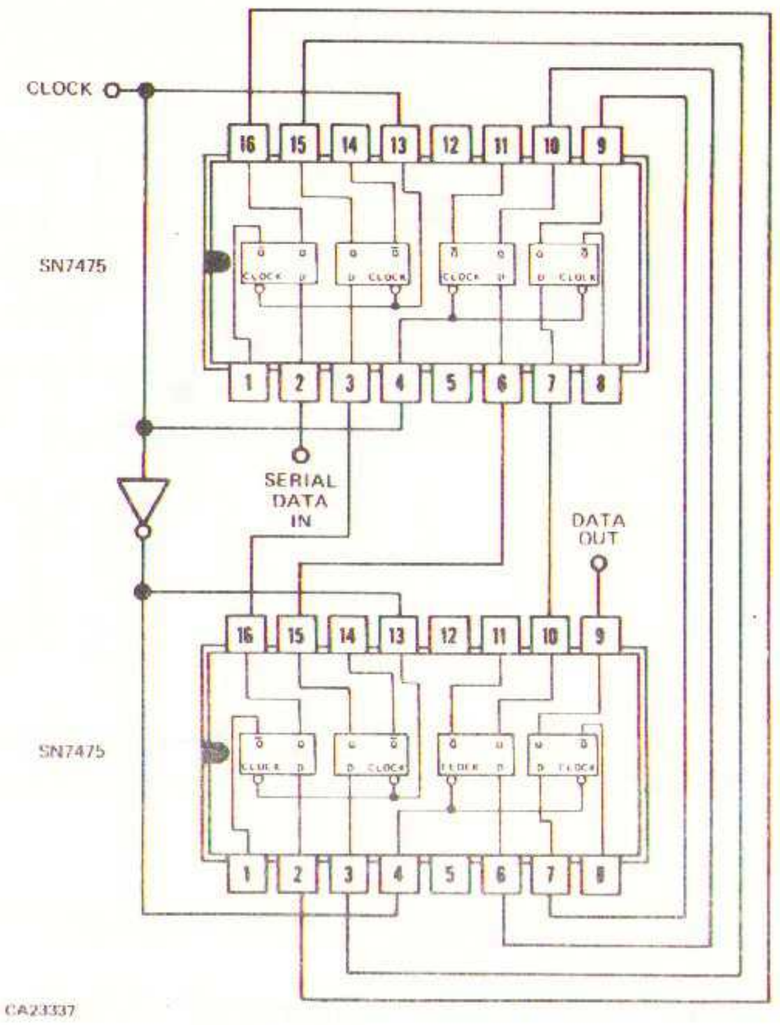


Figure 11C. 4-Bit Serial Shift Register Using SN74

H. ADDRESSABLE REGISTER FILE USING SN7475'S

The SN7475 quad latch may be used as a four-bit-per-byte addressable storage register as shown in Figure 11D. The addressing is achieved with the SN7442 three-to-eight or four-to-ten-line decoder. A 4-bit byte is entered into the input register and can then be transferred to any of eight output registers. More output registers may be added if additional SN7442's are used (2^n registers for n address lines). Furthermore, if additional input registers are included, the output registers may be extended to handle bytes in multiples of four bits. This example is very useful for decimal serial-by-character to parallel conversion.

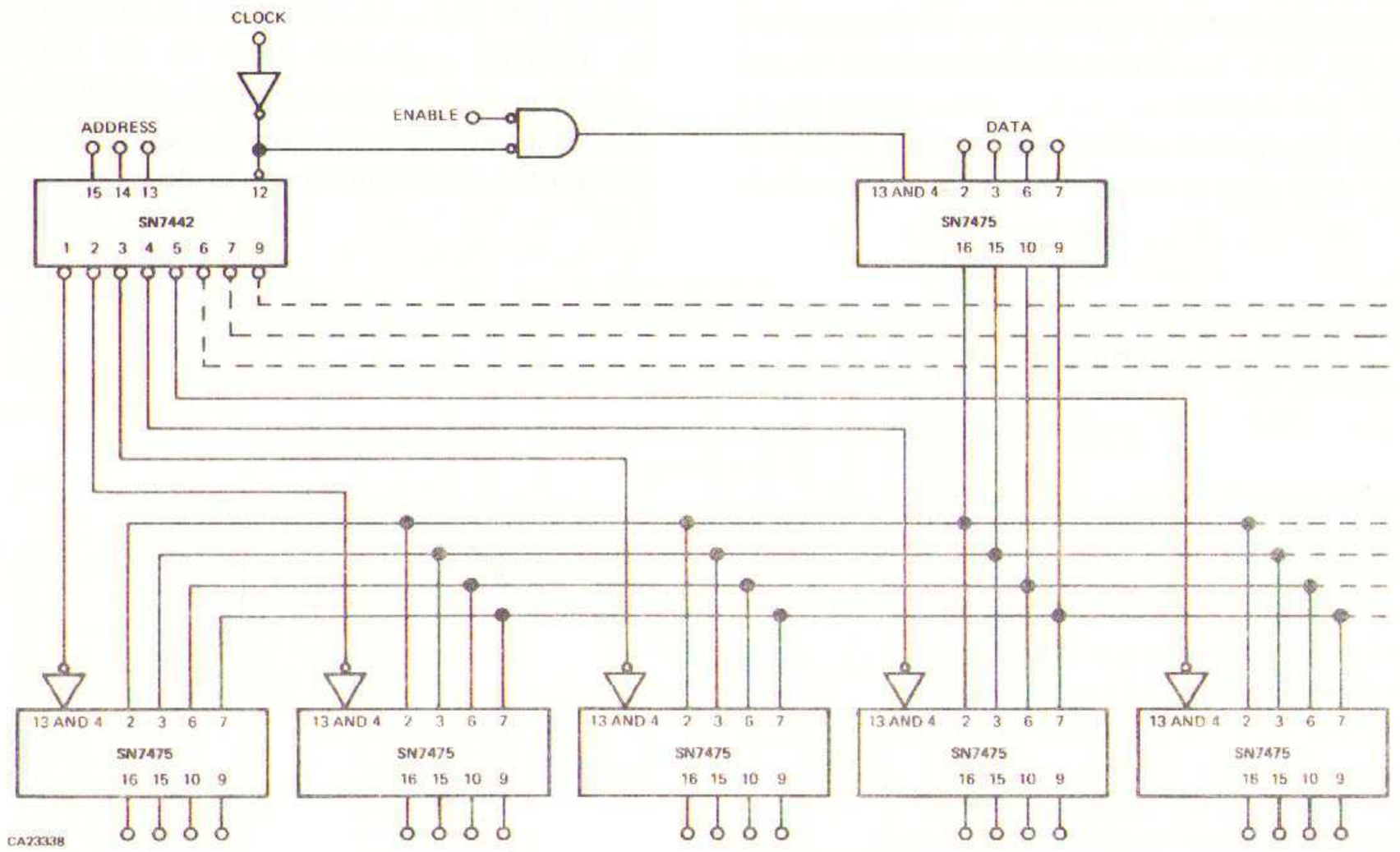


Figure 11D. 4-Bit-Per-Byte Addressable Register File Using SN7475's

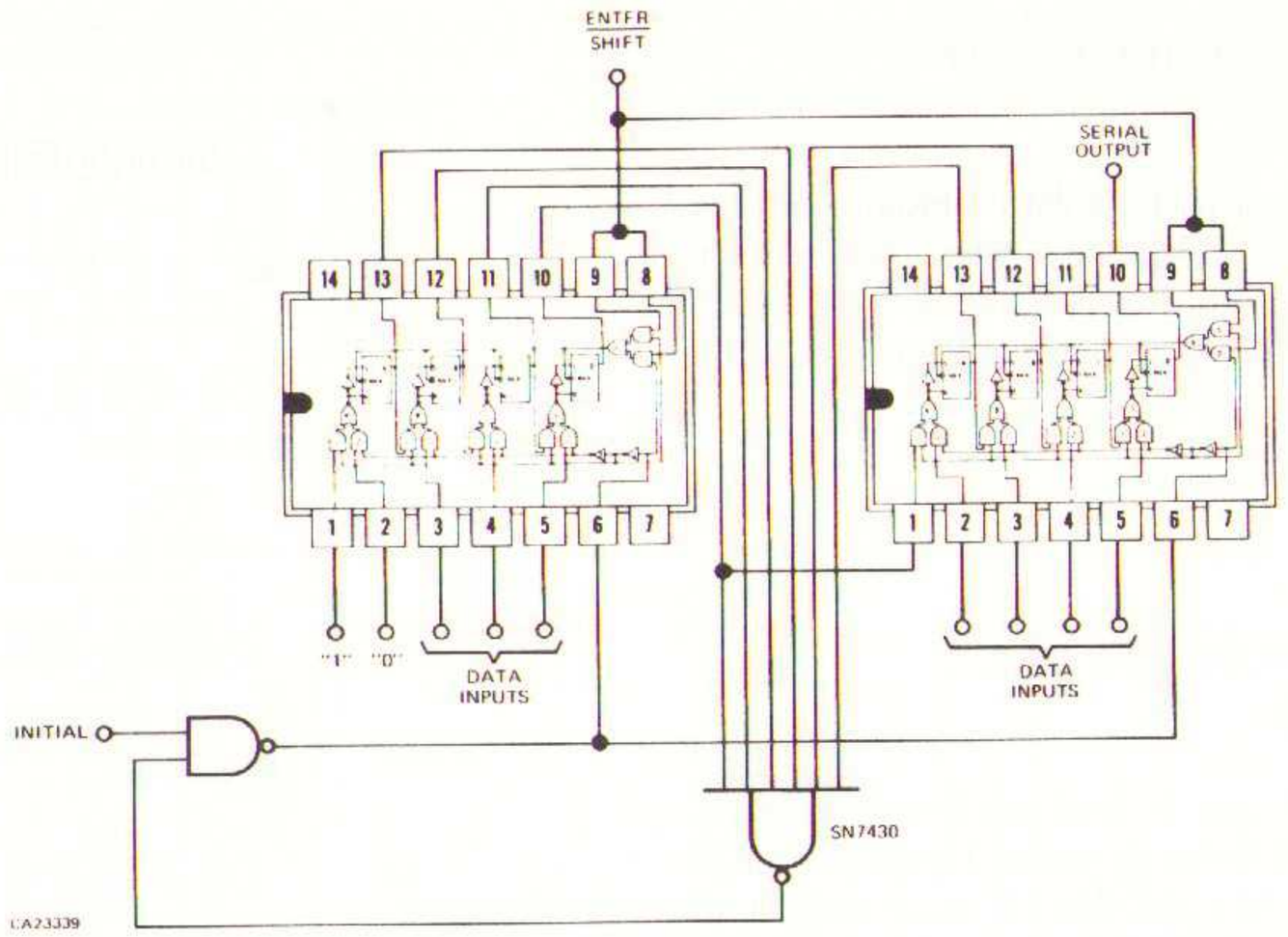


Figure 11E. 7-Bit Parallel-To-Serial Converter Using SN7495's

J. PARALLEL-TO-SERIAL CONVERTER USING SN7495'S

The parallel-to-serial converter in Figure 11E accepts parallel data in groups of 7 bits at the data inputs of the SN7495. Together with the data, a logical "0" is entered into the first stage by applying a negative pulse at the INITIAL input. The INITIAL input has to be used only once at the beginning of the conversion to set the registers in a known state. Then the data is shifted out in series and logical "ones" are entered in series. After seven clock pulses, the data has all been shifted out, and the register is full of "ones." This state is decoded by the SN7430, which initiates a new 7-bit conversion cycle without requiring a new INITIAL pulse.

K. SERIAL-TO-PARALLEL CONVERTER USING SN7495'S

Figure 11F shows SN7495's in a serial-to-parallel converter. By applying a positive pulse to the INITIAL line, the register is set to a known state (D1000000), where D is the first data bit. When the "one" is shifted to the last stage of the register, a new conversion cycle is initiated.

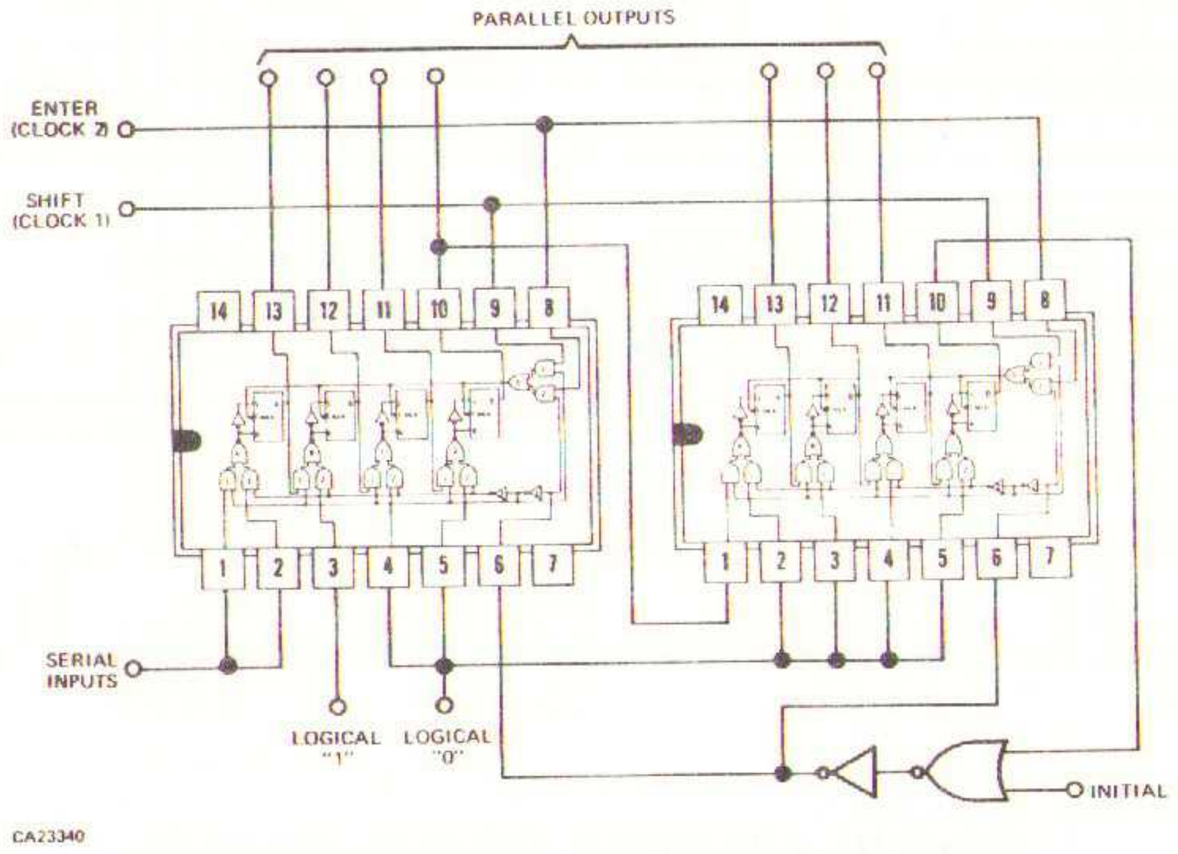


Figure 11F. 7-Bit Serial-To-Parallel Converter Using SN7495's

IV. SERIES 74 BINARY RIPPLE-COUNTER DESCRIPTIONS

A. DECADE COUNTER SN7490

This decade counter consists of four master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. See Figure 12. Gated, direct-reset lines are provided to inhibit count inputs and return all outputs to a logical zero or to a binary-coded-decimal (BCD) count of nine. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary-coded-decimal decade counter, the B input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table. See Figure 13. In addition to a conventional zero reset, inputs are provided to reset a BCD 9 count for nine's complement decimal applications.

2. If a symmetrical divide-by-ten count is desired for frequency synthesizers, or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the B input and a divide-by-ten square wave is obtained at output A. See Figure 13.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The B input is used to obtain binary divide-by-five operation at the B, C, and D outputs. See Figure 13. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

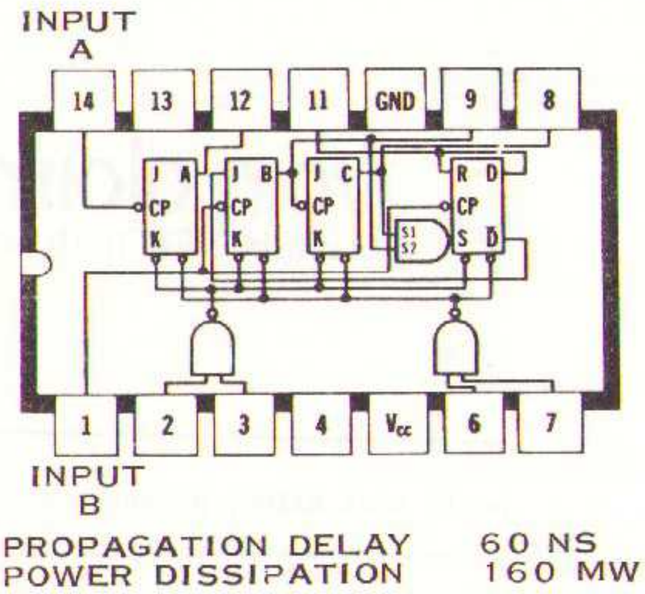


Figure 12. Decade Counter

MODE 1 (BCD)				MODE 2 (SYMMETRICAL DIVIDE-BY-TEN)				MODE 3 (DIVIDE-BY-FIVE)		
A	B	C	D	A	B	C	D	B	C	D
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	1	0	0
0	1	0	0	0	0	1	0	0	1	0
1	1	0	0	0	1	1	0	1	1	0
0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	1	0	0	0			
0	1	1	0	1	1	0	0			
1	1	1	0	1	0	1	0			
0	0	0	1	1	1	1	0			
1	0	0	1	1	0	0	1			

Figure 13. Decade Counter Truth Tables

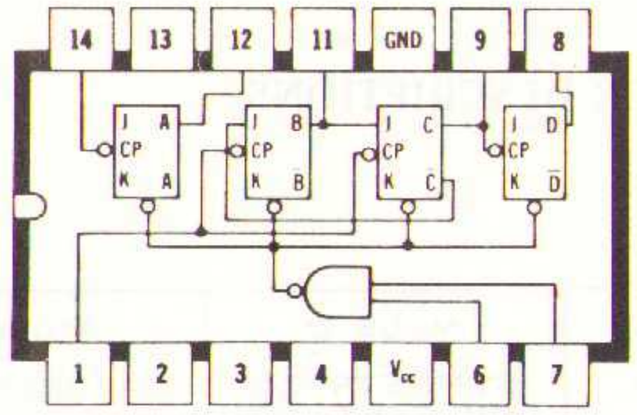
B. DIVIDE-BY-TWELVE COUNTER SN7492

This 4-bit binary counter consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. See Figure 14. A gated, direct-reset line can inhibit the count inputs and simultaneously return the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in three modes:

1. When used as a divide-by-twelve counter, output A may be externally connected to input BC. Then input count pulses are applied to input A. Simultaneous divisions of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the mode 1 truth table. See Figure 15.

2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneous frequency divisions of three and six are available at the C and D outputs. See Figure 15. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

3. Another divide-by-twelve code is available if output D is externally connected to input A. The input count pulses are then applied to input BC. Simultaneous frequency divisions of 3, 6, and 12 are available at the C, D, and A outputs as shown. See Figure 15.



PROPAGATION DELAY 60 NS
POWER DISSIPATION 160 MW

Figure 14. Divide-by-12 Counter

MODE 1 (DIVIDE–BY–12)				MODE 2 (DIVIDE–BY–6)			MODE 3 (DIVIDE–BY–12)			
A	B	C	D	B	C	D	A	B	C	D
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	0	0	1	0
1	1	0	0	0	0	1	0	0	0	1
0	0	1	0	1	0	1	0	1	0	1
1	0	1	0	0	1	1	0	0	1	1
0	0	0	1				1	0	0	0
1	0	0	1				1	1	0	0
0	1	0	1				1	0	1	0
1	1	0	1				1	0	0	1
0	0	1	1				1	1	0	1
1	0	1	1				1	0	1	1

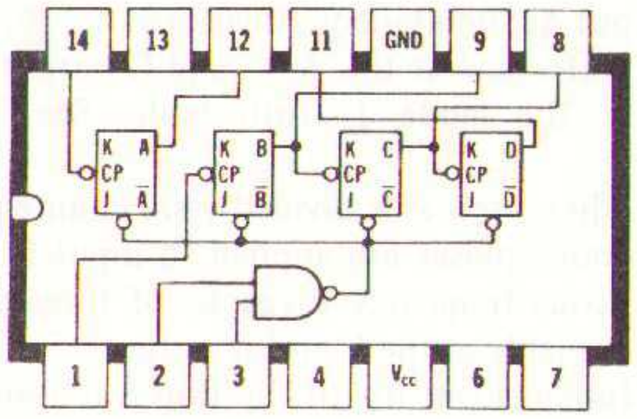
Figure 15. Divide-by-12 Counter Truth Tables

C. 4-BIT BINARY COUNTER SN7493

This 4-bit binary counter consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. See Figure 16. A gated, direct-reset line returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8 and 16 are performed at the A, B, C, and D outputs as shown in the truth table. See Figure 17.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. See Figure 17. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.



PROPAGATION DELAY 75 NS
POWER DISSIPATION 160 MW

Figure 16. 4-Bit Binary Counter

MODE 1 (DIVIDE–BY–16)				MODE 2 (DIVIDE–BY–8)		
D	C	B	A	B	C	D
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	1	0
0	0	1	1	1	1	0
0	1	0	0	0	0	1
0	1	0	1	1	0	1
0	1	1	0	0	1	1
0	1	1	1	1	1	1
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

Figure 17. 4-Bit Binary Counter Truth Tables

V. DIVIDE-BY-N RIPPLE COUNTERS (N=CYCLE LENGTH)

A. COUNTERS USING SN7490, SN7492, SN7493

For some counting applications, the SN7490, SN7492, SN7493 ripple counters may be modified to change the count cycle. By decoding any desired cycle length at the outputs of the A, B, C, D flip-flops and feeding this signal to the asynchronous clear inputs, the counter can be made to adopt a shortened cycle. The maximum frequency in this mode is determined by the restriction that the clock should not go low for approximately 40 nanoseconds after the counter has been reset to zero. See Figure 18. The outputs which are in a logical 1 state at the count (N) are fed into the $R_{0(1)}$ and $R_{0(2)}$ inputs. The counter will then reset to the all zero state when the count (N) appears at these outputs. According to the count cycle (N), voltage spikes may appear on some output lines. See output B waveform, Figure 19. When the outputs are to be decoded, a strobe gate should be provided to inhibit false output data. When the outputs are not equally and heavily loaded, timing difficulties may be encountered at the temperature extremes. Buffering outputs with the configuration shown in Figure 20 will prevent these difficulties.

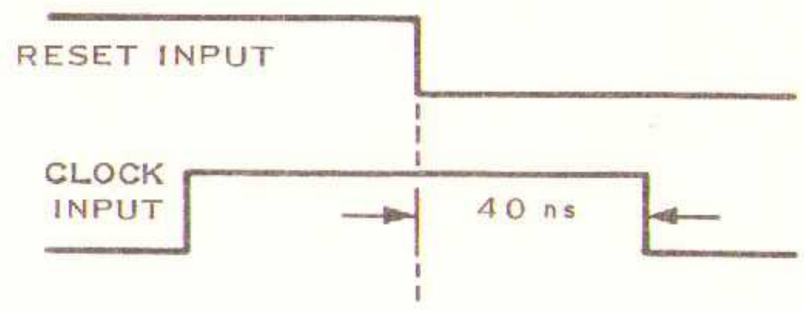
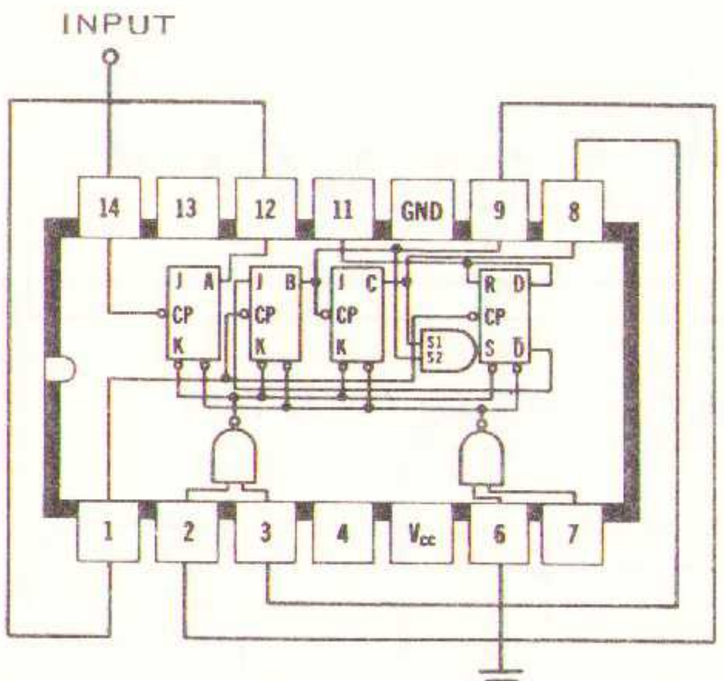


Figure 18. Typical Reset Timing Requirement

For larger division ratios in BCD code, two or more SN7490's may be cascaded. BCD numbers with no more than two "ones" in their sequence do not require external gates. See Figure 21. Some other numbers which do not require external gates are: 11, 12, 14, 18, 21, 22, 24, 28, 41, 42, 44, 48, 81, 82, 84, 88 . . . (and others).

All other division ratios in BCD can be achieved with two SN7490's, one NAND gate, and one inverter. See Figure 22.



CLOCK PULSE	OUTPUT			
	A	B	C	D
t_n	0	0	0	0
t_{n+1}	1	0	0	0
t_{n+2}	0	1	0	0
t_{n+3}	1	1	0	0
t_{n+4}	0	0	1	0
t_{n+5}	1	0	1	0
t_{n+6}	0/0	1/0	1/0	0/0

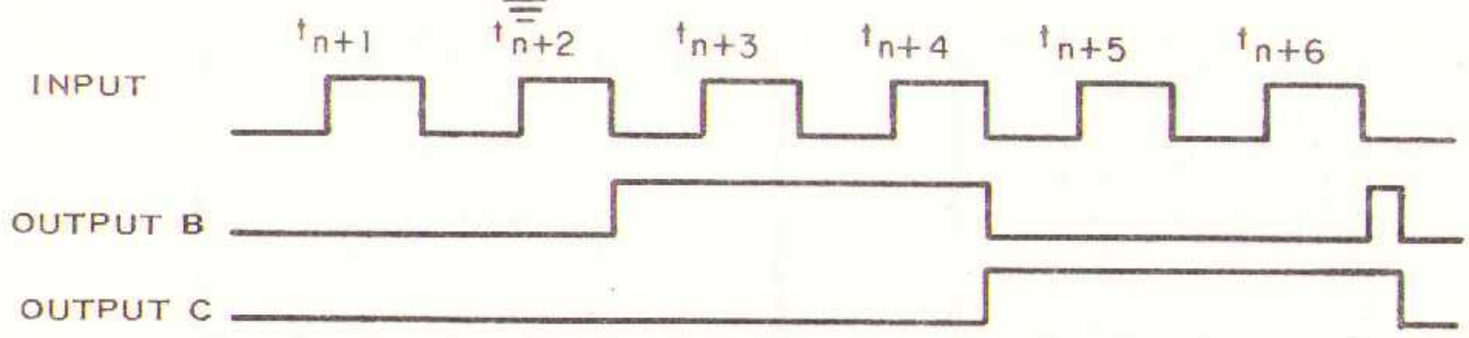


Figure 19. Binary Divide-by-6 Ripple Counter Using SN7490

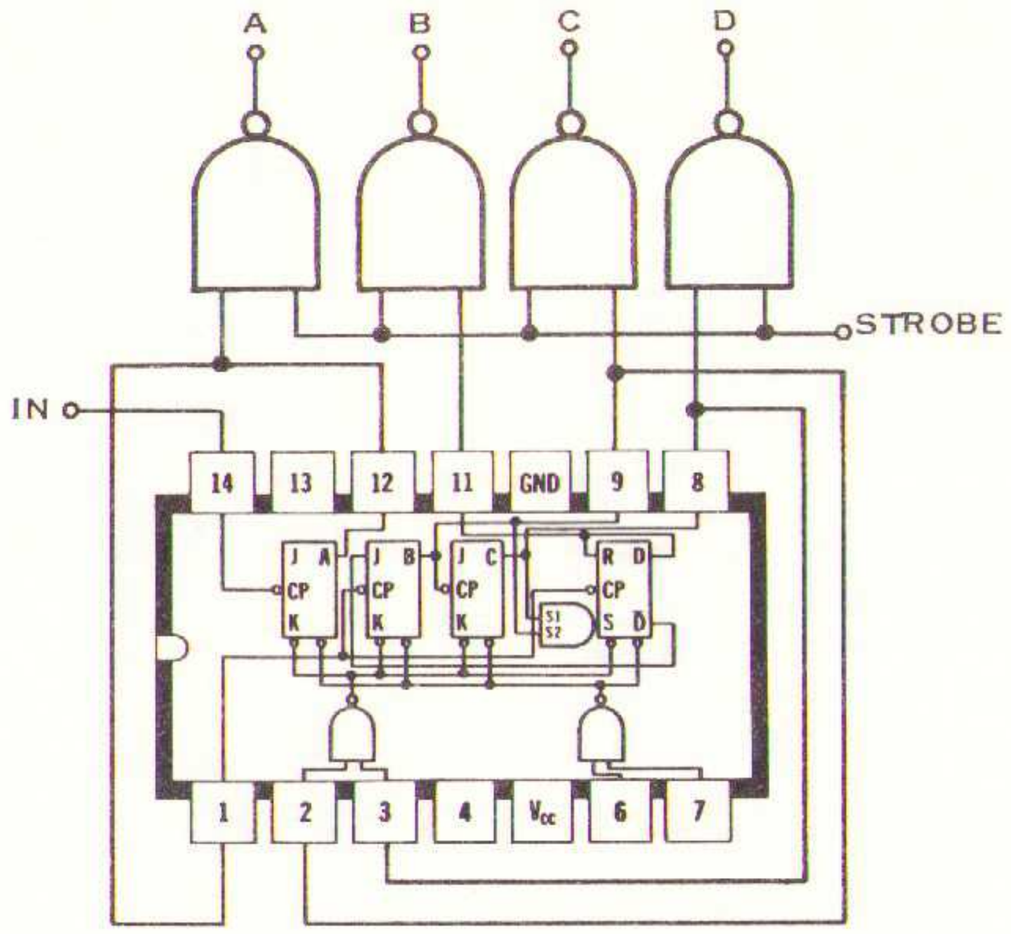


Figure 20. Binary Divide-by-6 Ripple Counter Using SN7490 (Buffered Outputs)

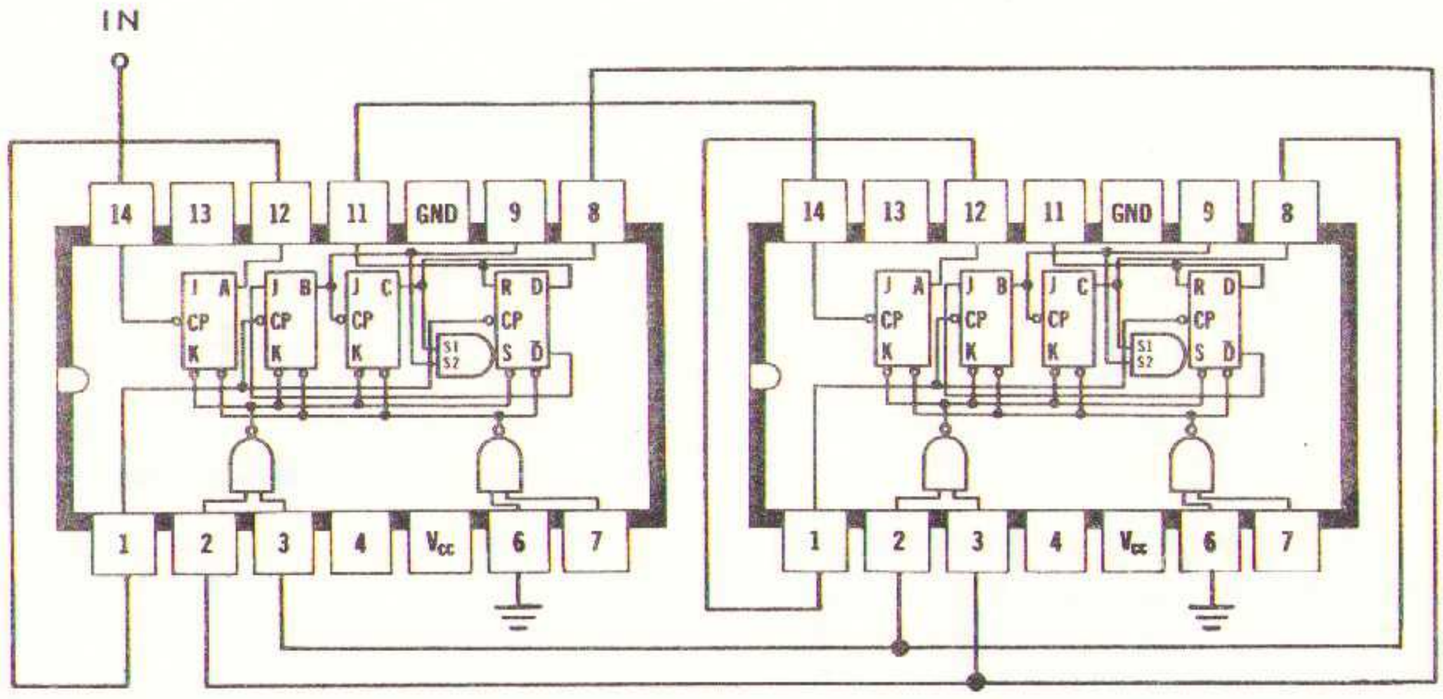


Figure 21. BCD Divide-by-44 Ripple Counter Using Two SN7490's

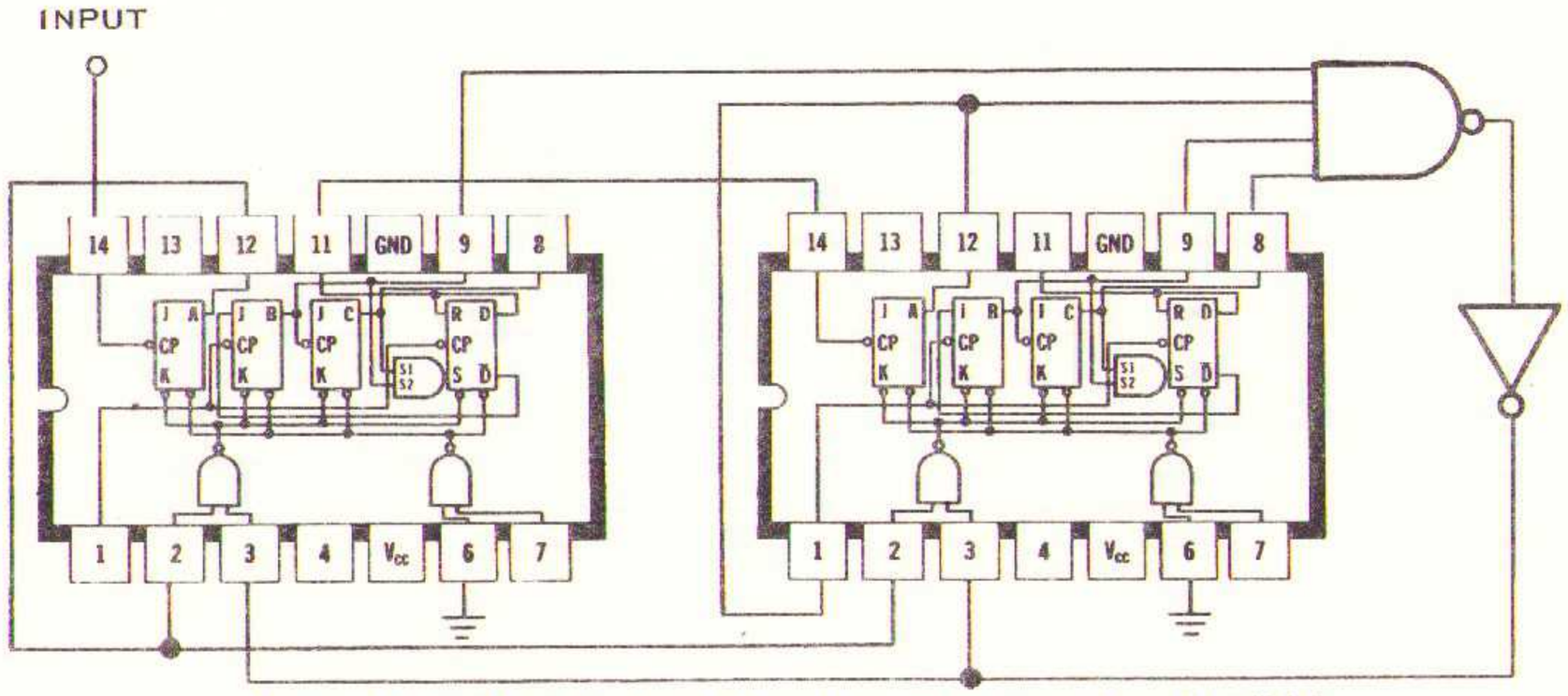


Figure 22. BCD Divide-by-73 Ripple Counter Using Two SN7490's

The following examples illustrate use of the SN7492 and SN7493 for various cycle length.

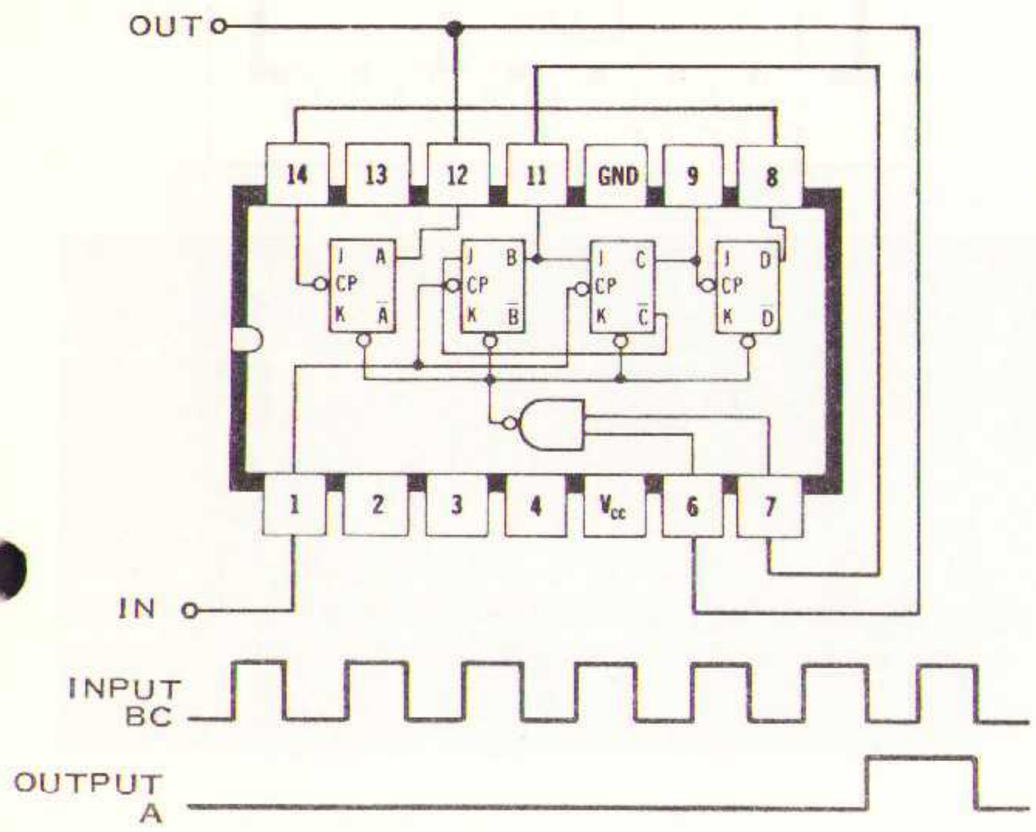


Figure 23. Divide-by-7 Ripple Counter Using SN7492

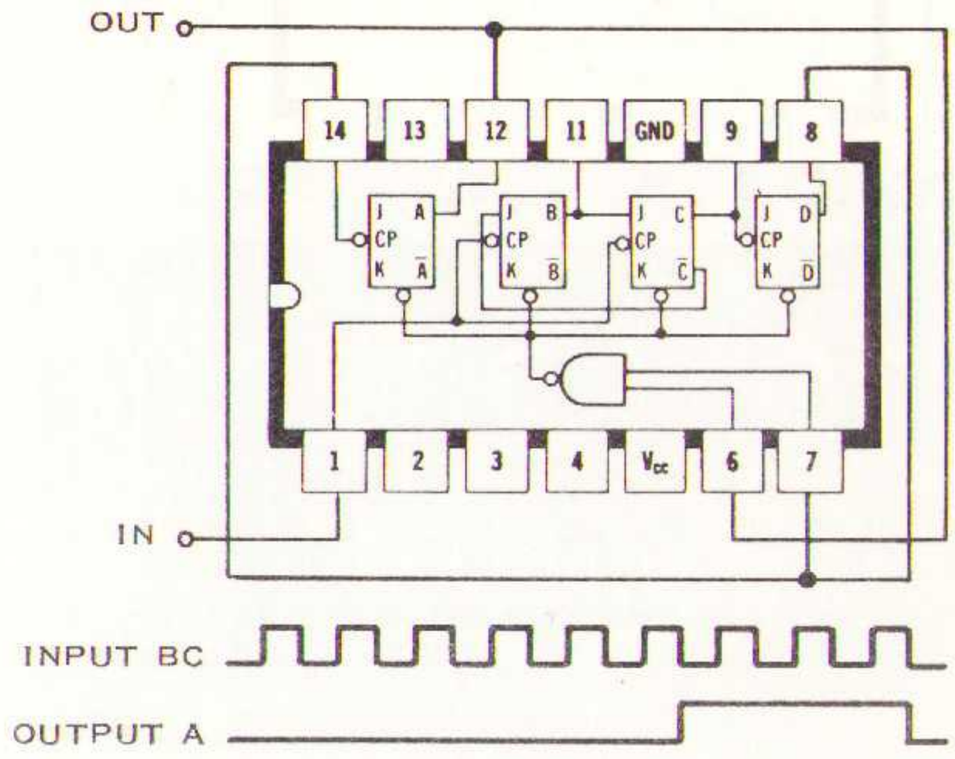


Figure 24. Divide-by-9 Ripple Counter Using SN7492

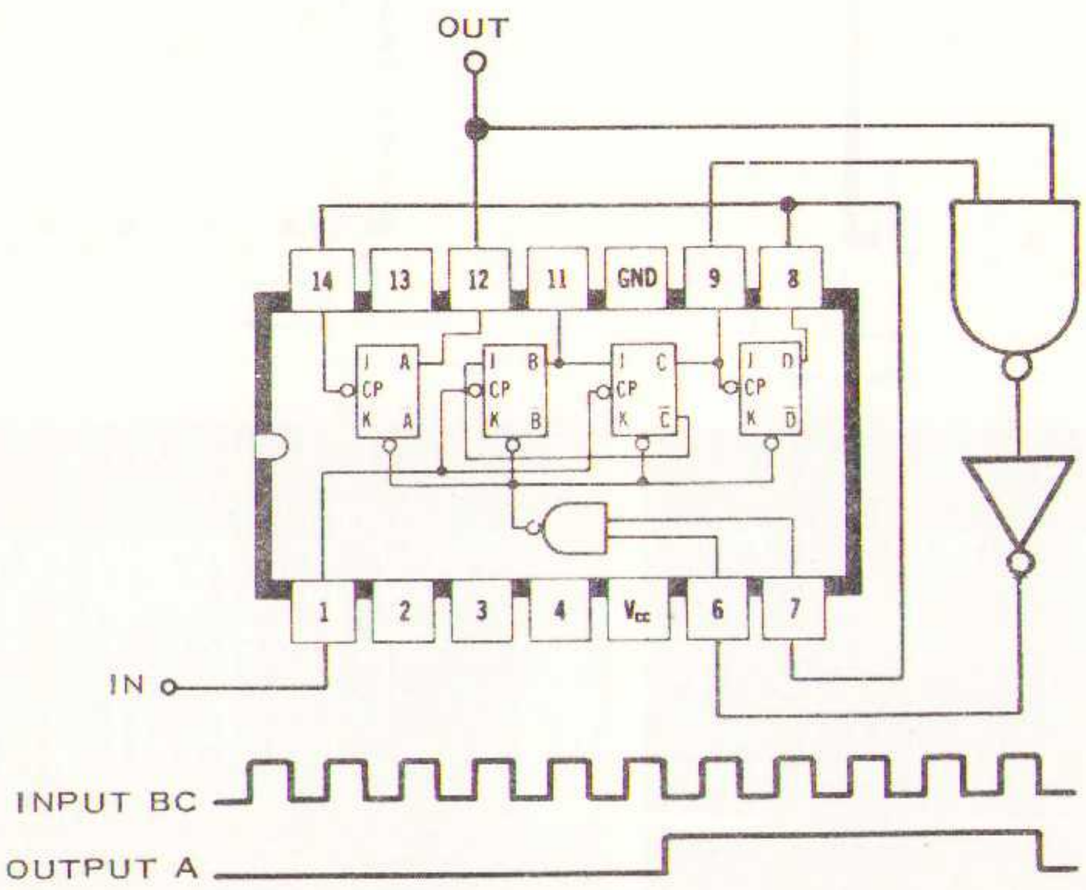


Figure 25. Divide-by-11 Ripple Counter Using SN7492

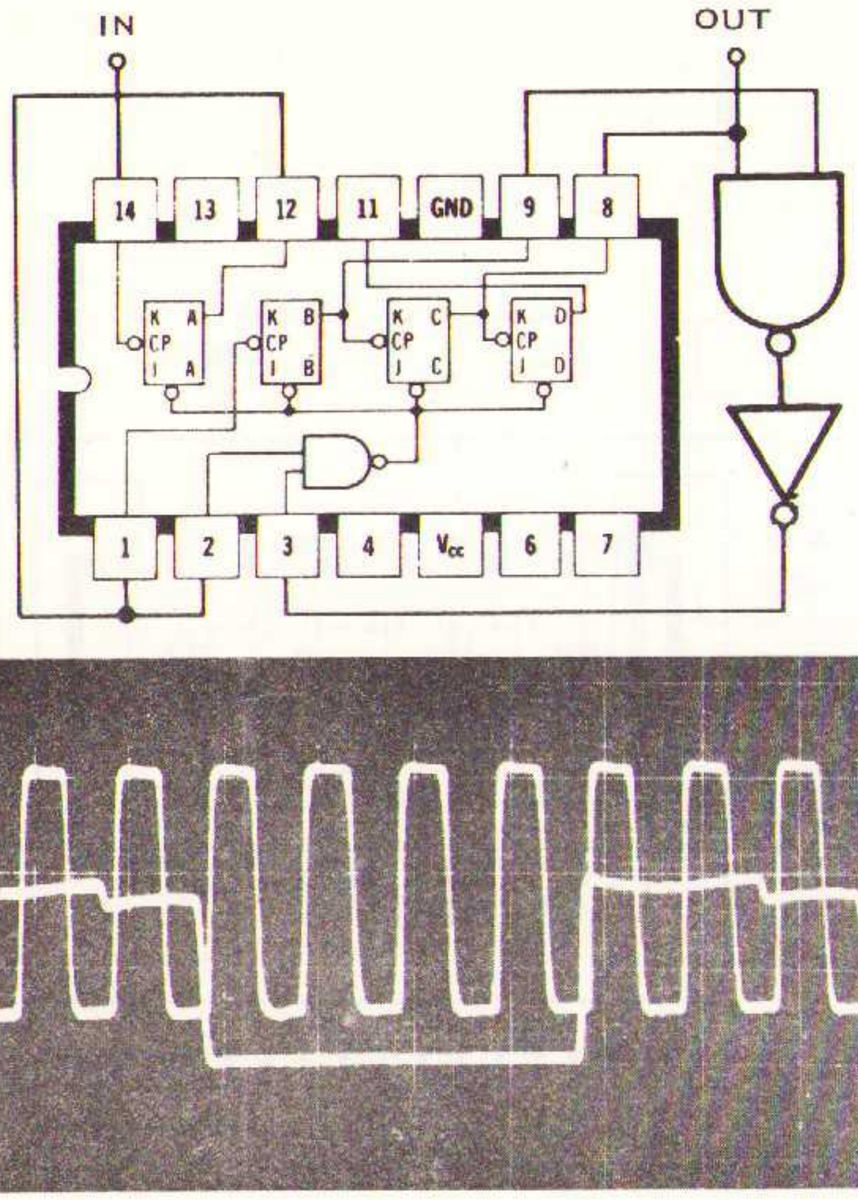


Figure 26. Binary Divide-by-7 Ripple Counter Using SN7493

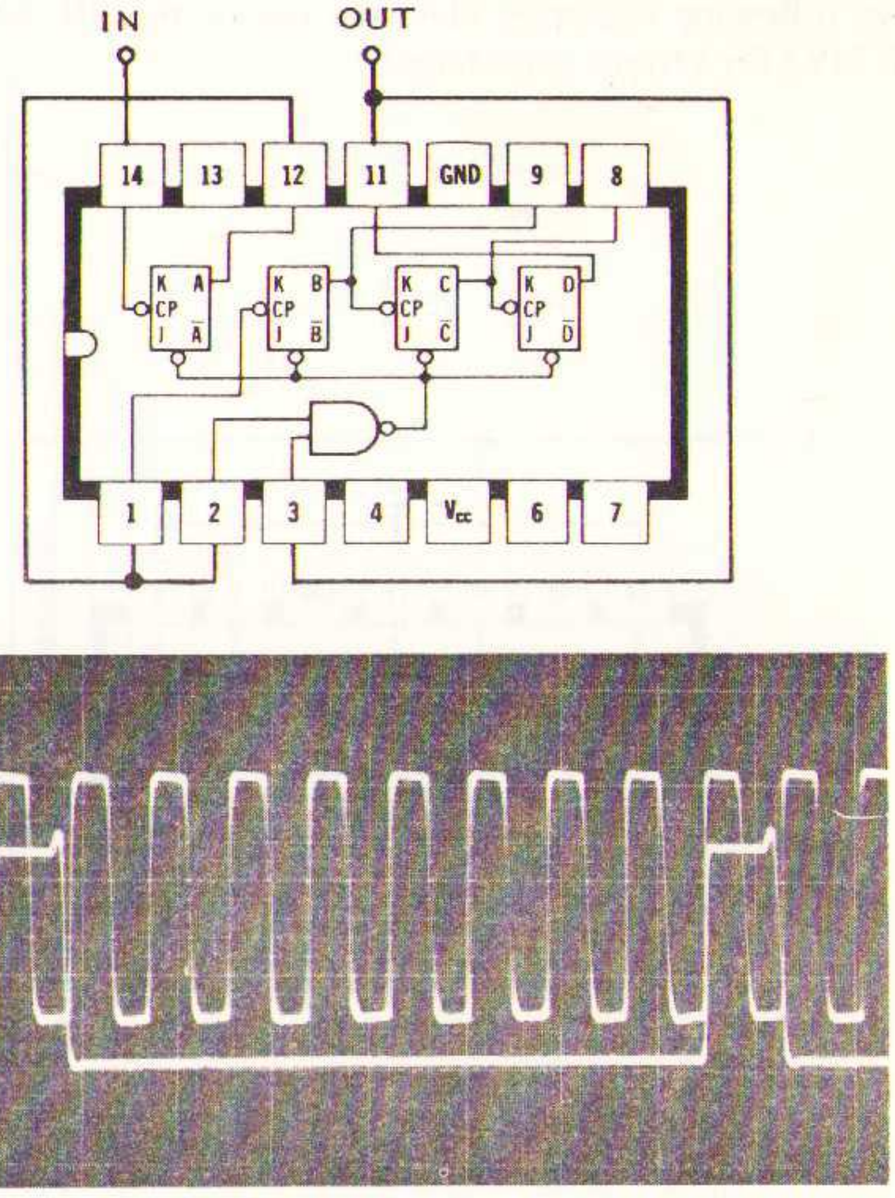


Figure 27. Binary Divide-by-9 Ripple Counter Using SN7493

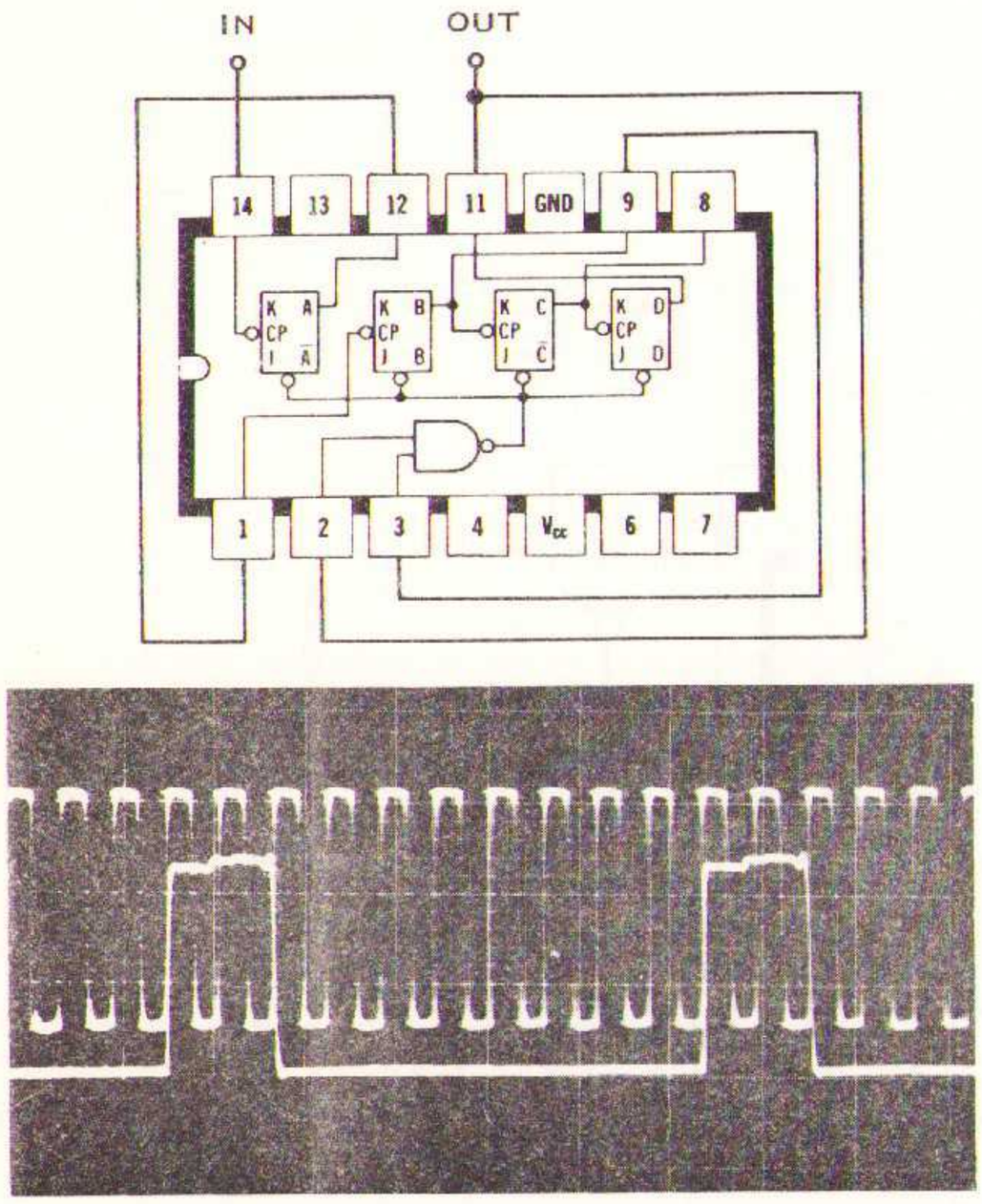


Figure 28. Binary Divide-by-10 Ripple Counter Using SN7493

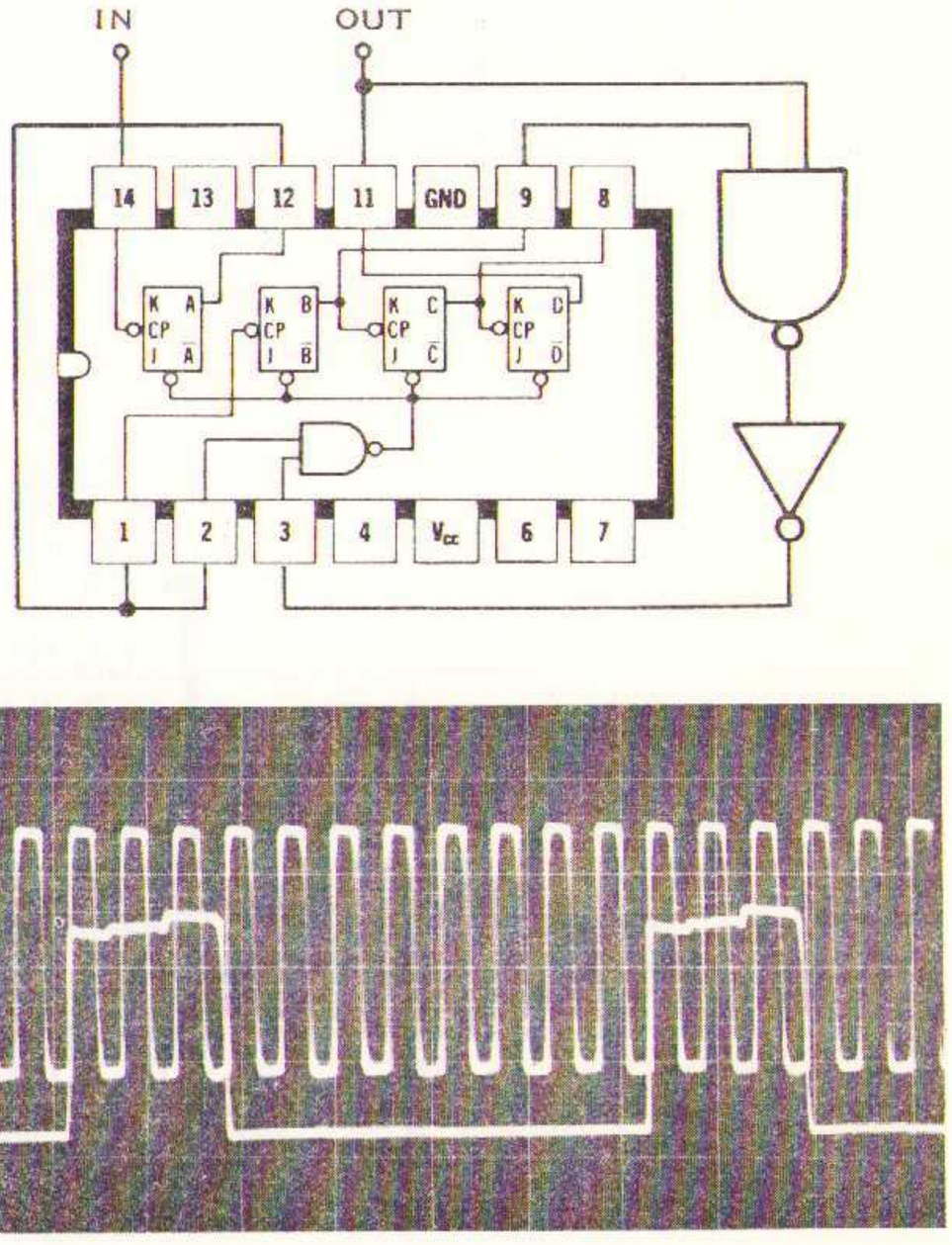
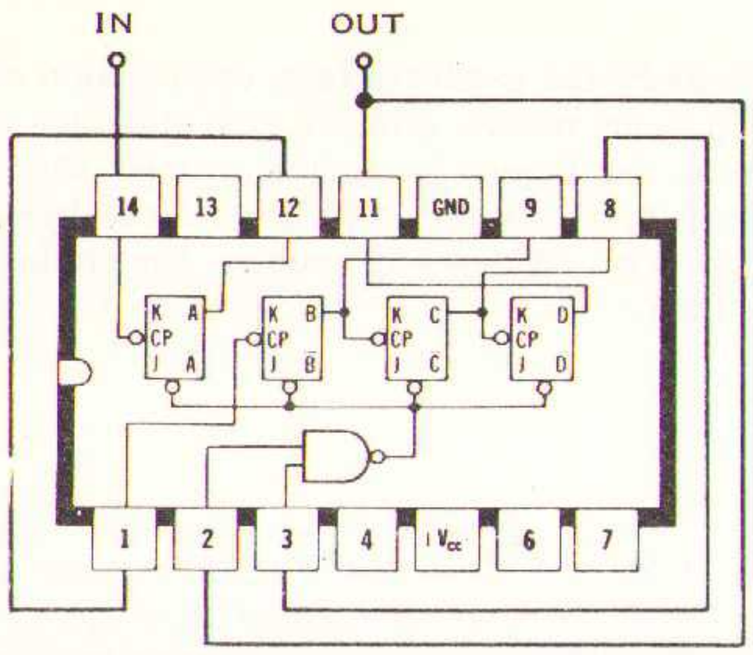


Figure 29. Binary Divide-by-11 Ripple Counter Using SN7493



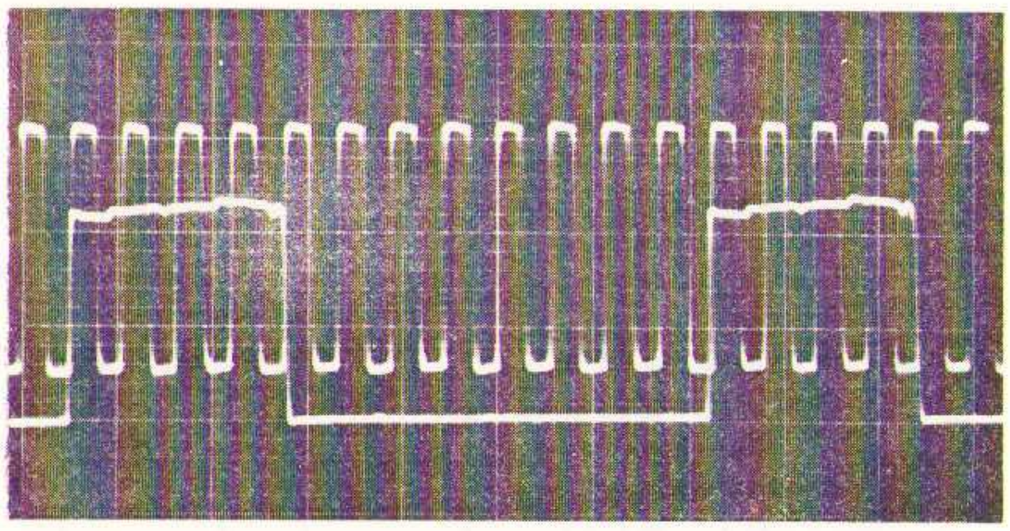
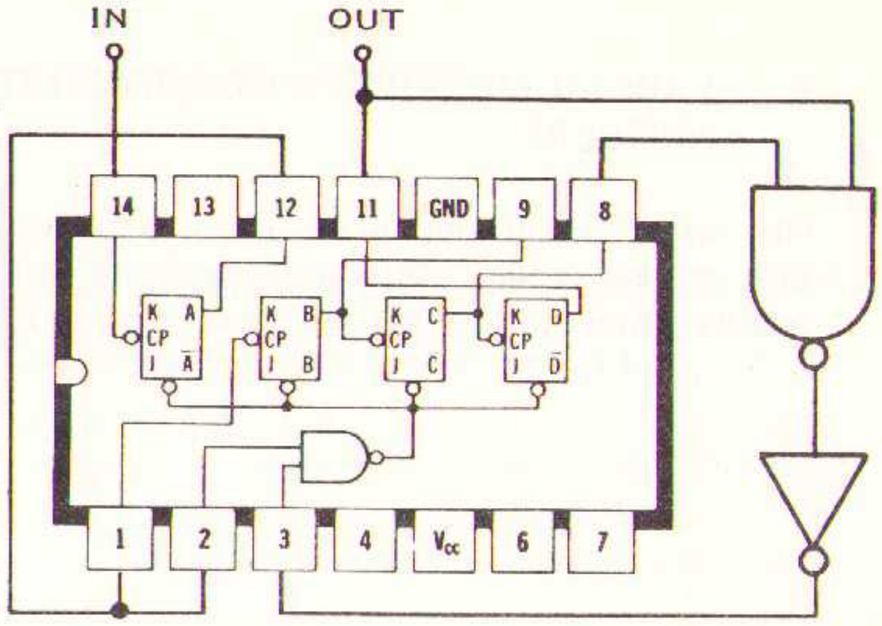


Figure 30. Binary Divide-by-12 Ripple Counter Using SN7493



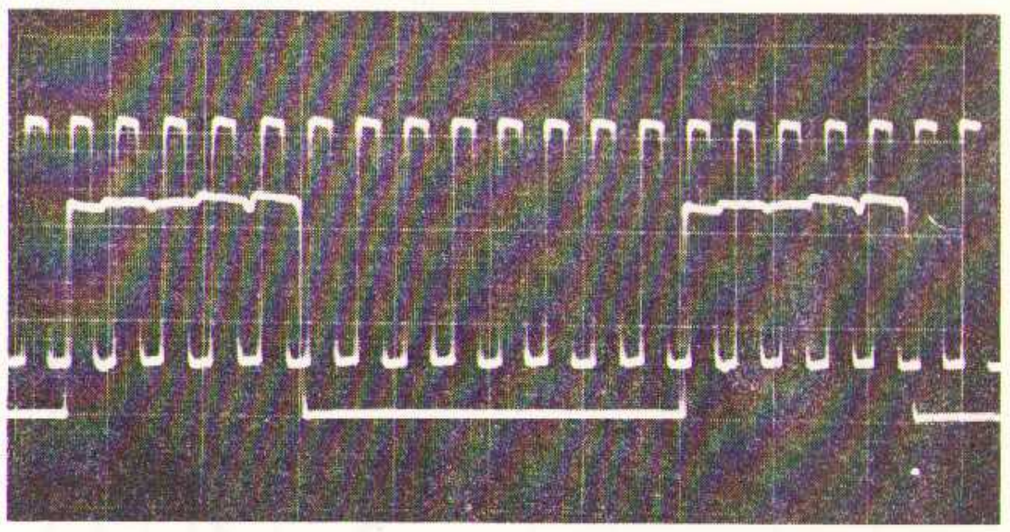
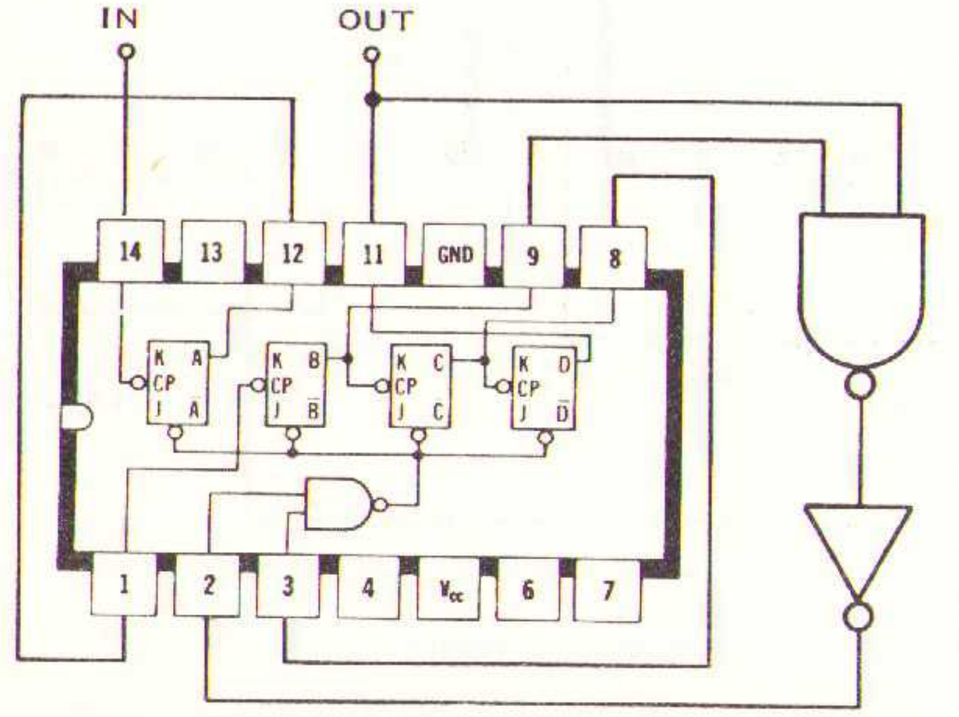


Figure 31. Binary Divide-by-13 Ripple Counter Using SN7493



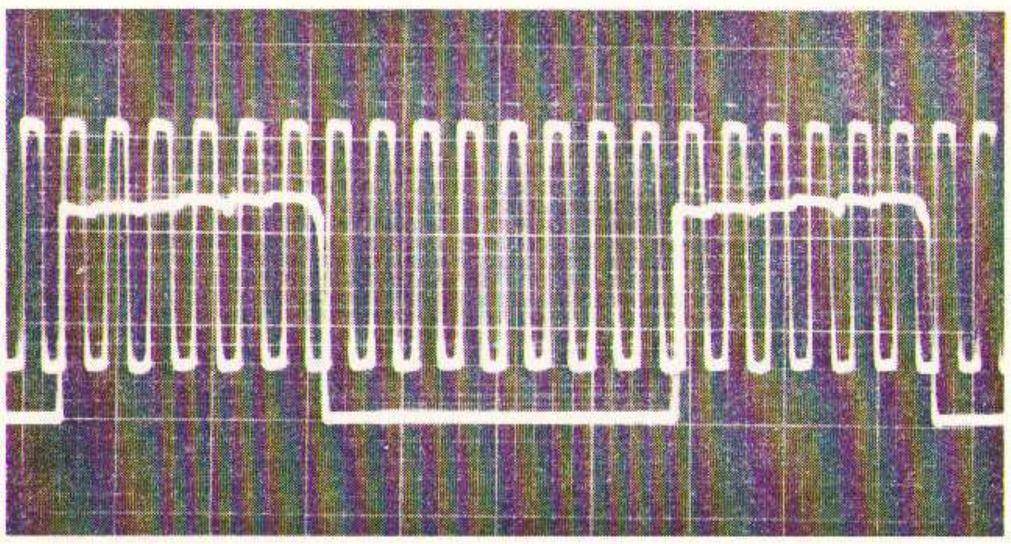
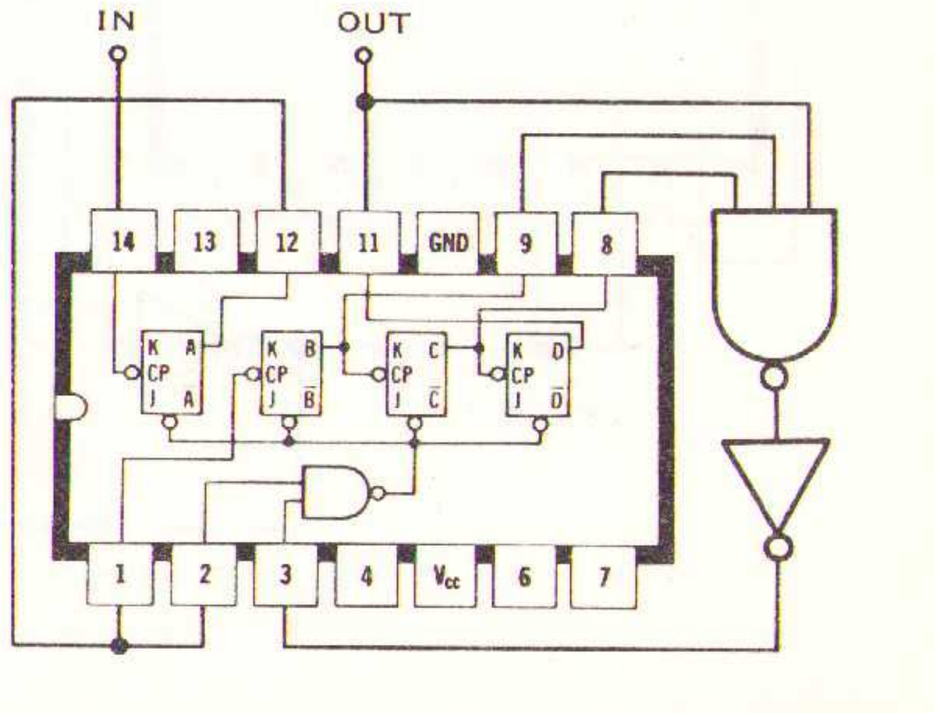


Figure 32. Binary Divide-by-14 Ripple Counter Using SN7493



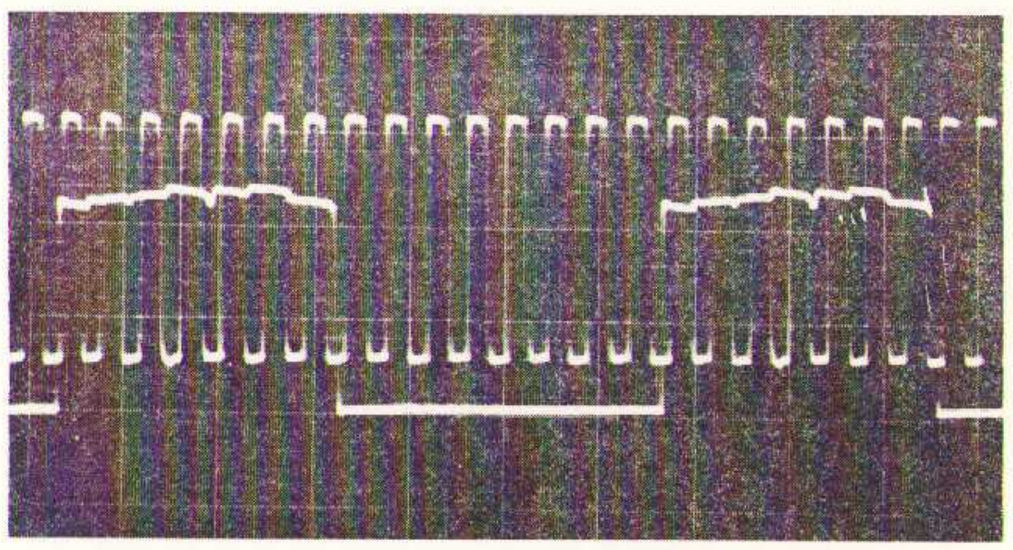


Figure 33. Binary Divide-by-15 Ripple Counter Using SN7493

B. LARGER FREQUENCY DIVISIONS USING PRIME NUMBERS

One very efficient method for larger frequency division ratios, as long as the code is not significant, is to count in a relative prime number system. Being able to divide by 2, 3, 4, 5 . . . . 13, 14, 15, with one counter makes it possible to divide by the product of any combination of those integers if they are relative prime to each other in a parallel arrangement. See Figure 34. In the example shown, stage 1 is a divide-by-7 counter, stage 2 is a divide-by-13 counter, and stage 3 is a divide-by-15 counter. The product (7 x 13 x 15) is 1365.

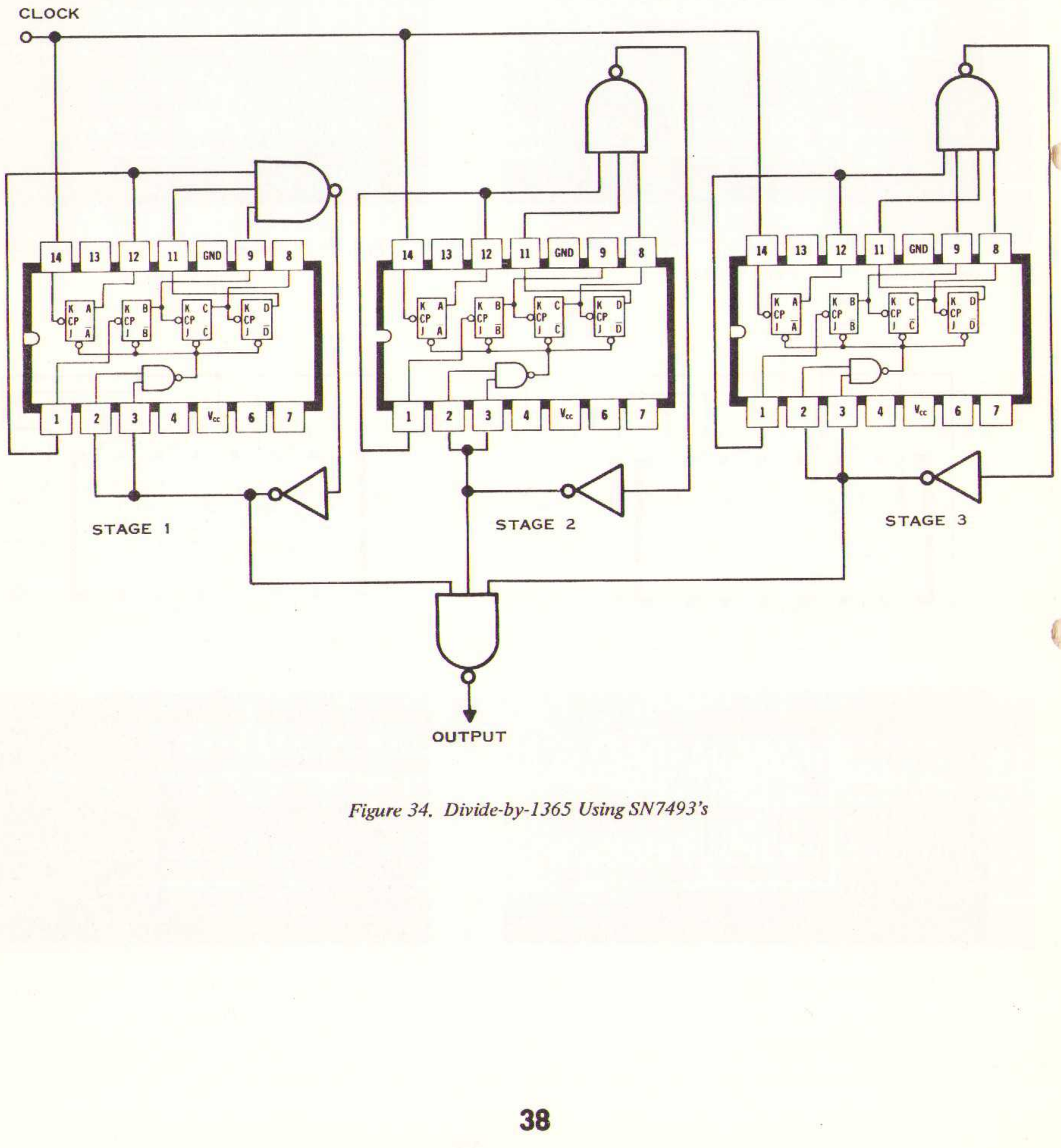


Figure 34. Divide-by-1365 Using SN7493's

VI. DIVIDE-BY-N RIPPLE COUNTERS USING RESET LATCH

A. 4-BIT COUNTER USING SN7490, SN7492, OR SN7493

Another application using the SN7490, SN7492, SN7493 divides by any number (N) in binary code. This circuit will operate over the operating temperature range of the devices used under full loading conditions, and is not dependent on the internal delay of the counter. The circuit uses 1 to 1-3/4 external gate packages. See Figure 35.

In this configuration, the last state of a count cycle sets a latch which clears the counter to the all zero state. The positive edge of the following clock pulse resets the latch. The negative edge of the same pulse initiates the new cycle.

Binary Divide-By-14 Ripple Counter (Example):

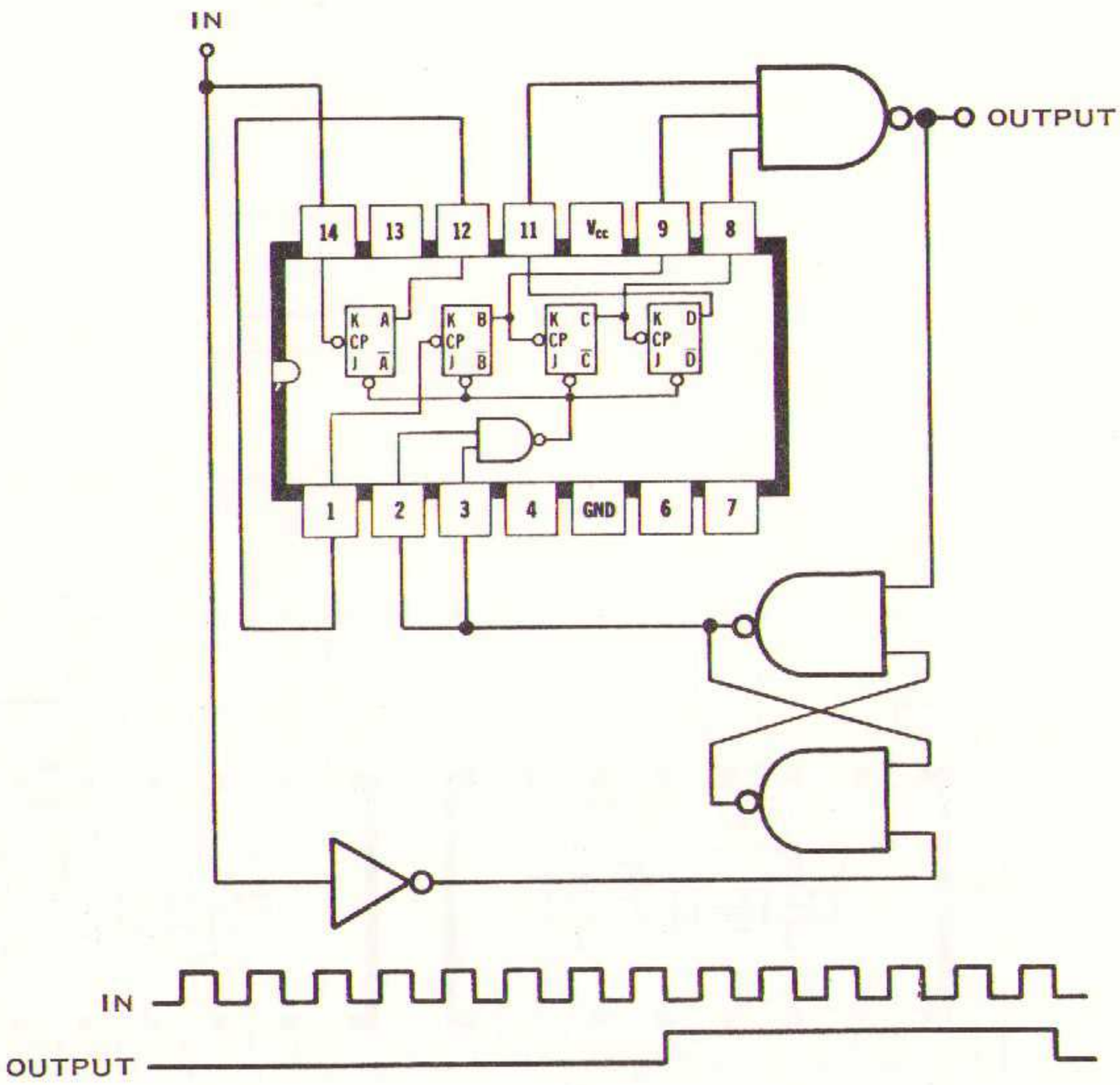


Figure 35. Divide-by-14 Binary Ripple Counter Using SN7493

B. 8-BIT COUNTER USING SN7493

A binary ripple counter which can count to any number (N) up to 256 can be built with two SN7493 counters and 1-3/4 gate packages. In the following examples, the "ones" of the binary word (N), which is the last binary count of the desired cycle length, are fed into the NAND gate. This particular counter recycles for every 153 input pulses.

A binary divide-by-153 ripple counter example is illustrated in Figure 36.

C. BCD DIVIDE-BY-89 COUNTER USING SN7490's

Some extended counts in the BCD code are possible by using multiple SN7490 decade counters. The following example utilizes two SN7490's and 1 external gate package. As in the two previous examples, the "ones" of the BCD word are fed into the NAND gate and the latch resets the two decade stages. This particular counter recycles for every 89 input pulses. See Figure 37.

Numerous other variations are possible especially when the symmetrical divide-by-10 mode of the SN7490 is considered.

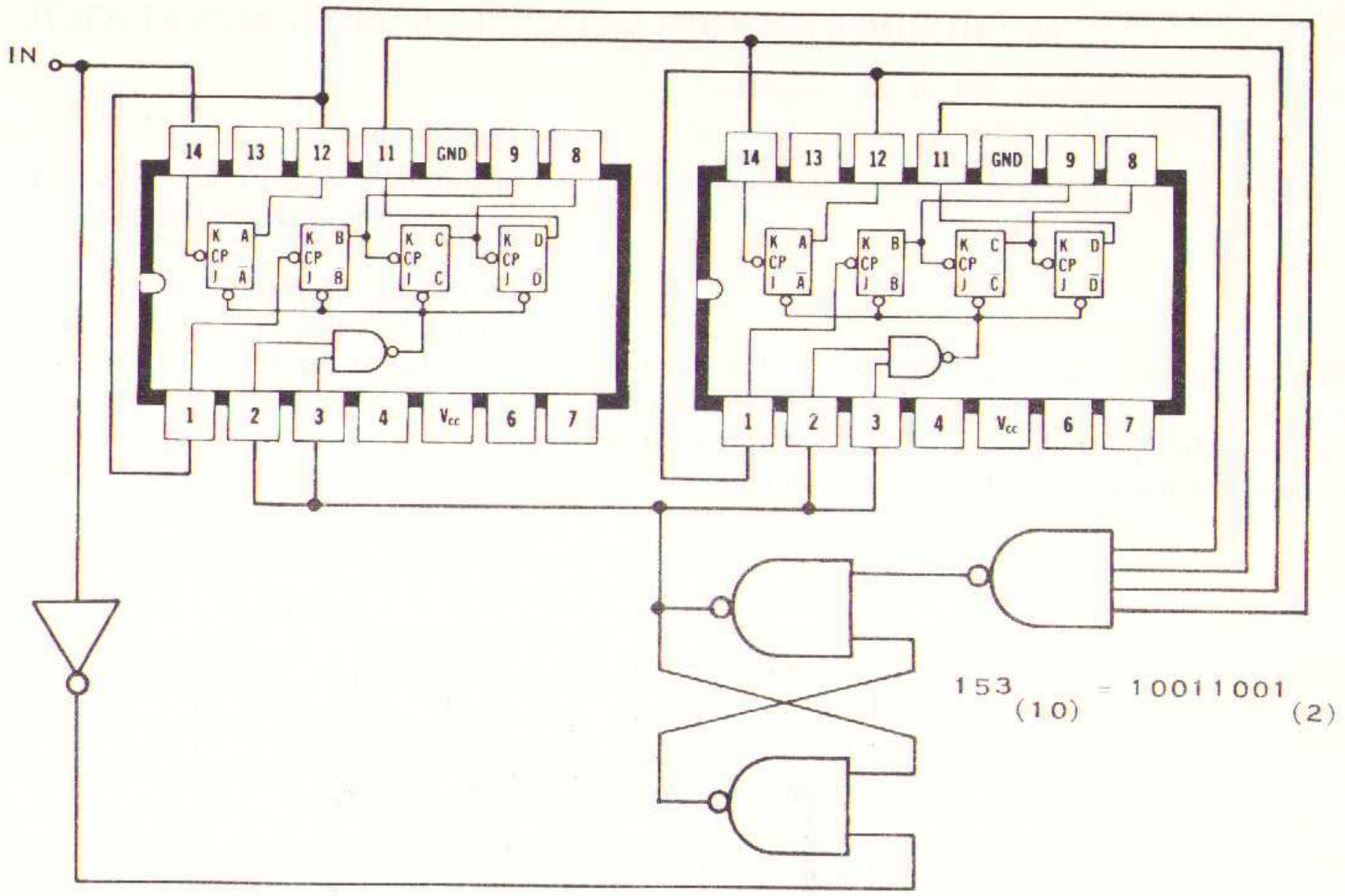


Figure 36. Divide-by-153 Binary Ripple Counter Using SN7493's

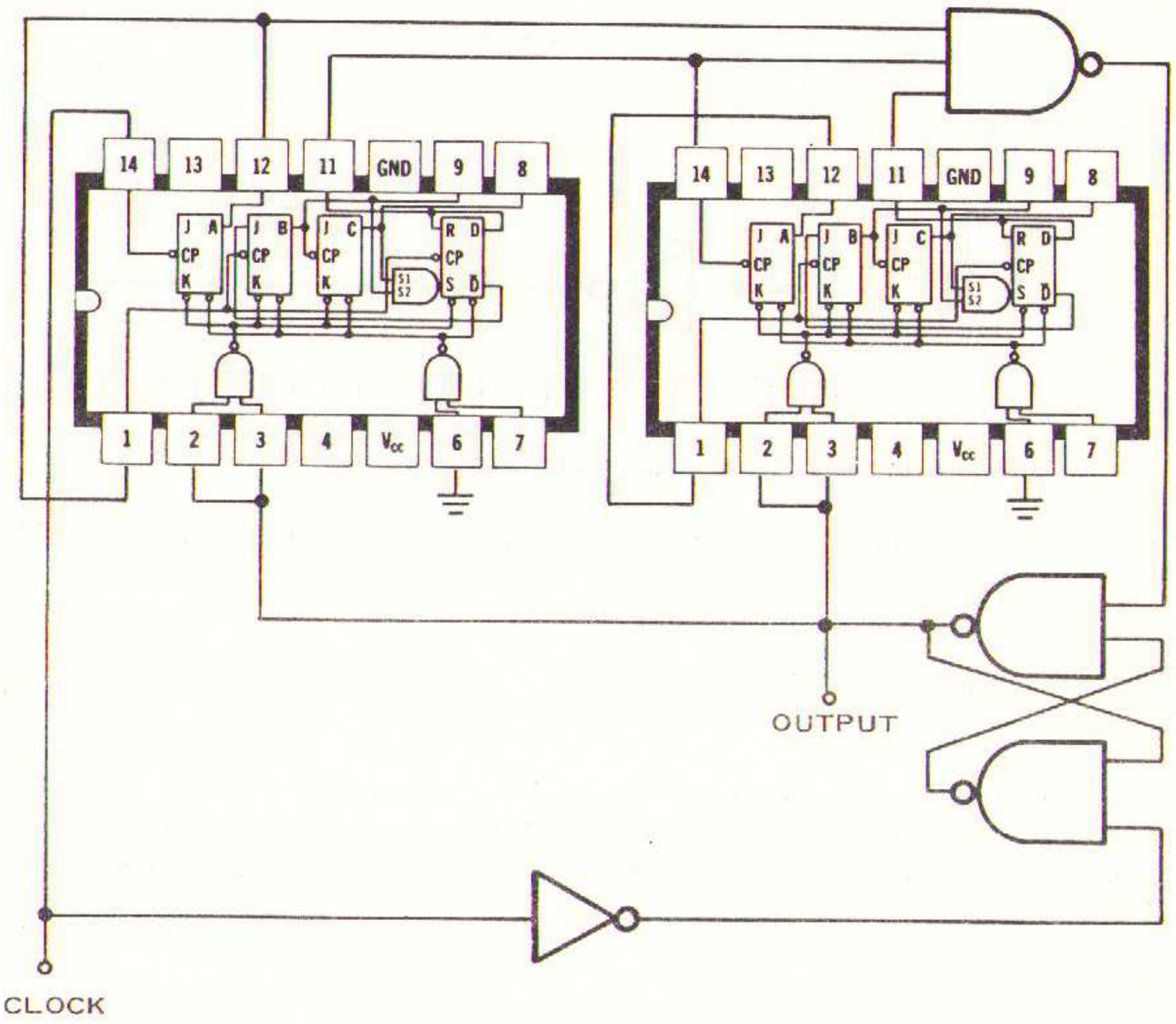


Figure 37. BCD Divide-by-89 Counter Using SN7490's

VII. BINARY DIVIDE-BY-N RIPPLE COUNTERS USING SINGLE OR DUAL FLIP-FLOPS

One other type of binary ripple counter using the asynchronous preset inputs to skip by binary counts can be very easily built for any cycle length using the following procedure:

1. If N is an integer and defined as the cycle length of the counter, then:

$$2^{n-1} \leq N \leq 2^n$$

with (n) = number of flip-flops required. If N is not a power of 2, find the next higher power of 2.

2. Connect all flip-flops as a ripple counter (outputs Q of stage (n) to clock input of stage (n + 1) and J to $\bar{Q}$, K to Q of each flip-flop.

3. Find the binary word N-1.

4. Connect all outputs of the flip-flops which are in the Q = 1 state at the count N - 1 as inputs to a NAND gate. Also feed the clock into the NAND gate.

5. Connect the NAND gate output to the preset inputs of all flip-flops for which Q = 0 at the state (N-1).

Here is how these counters work:

At the positive going edge of the N^{th} input pulse, all flip-flops are preset to the "1" state by the NAND gate. On the trailing edge of the same pulse, all flip-flops count to the "0" state. In other words, the counter recycles.

For N = 14 Counter:

1. $2^3 \leq 14 \leq 2^4$ It follows that n = 4 flip-flops required
2. Connect as an asynchronous binary counter
3. N = 14, binary: 01 1 1 (LSB most left)
4. (N - 1) = 13, Binary 1 0 1 1 (LSB most left)
5. Connect as shown in Figure 38.

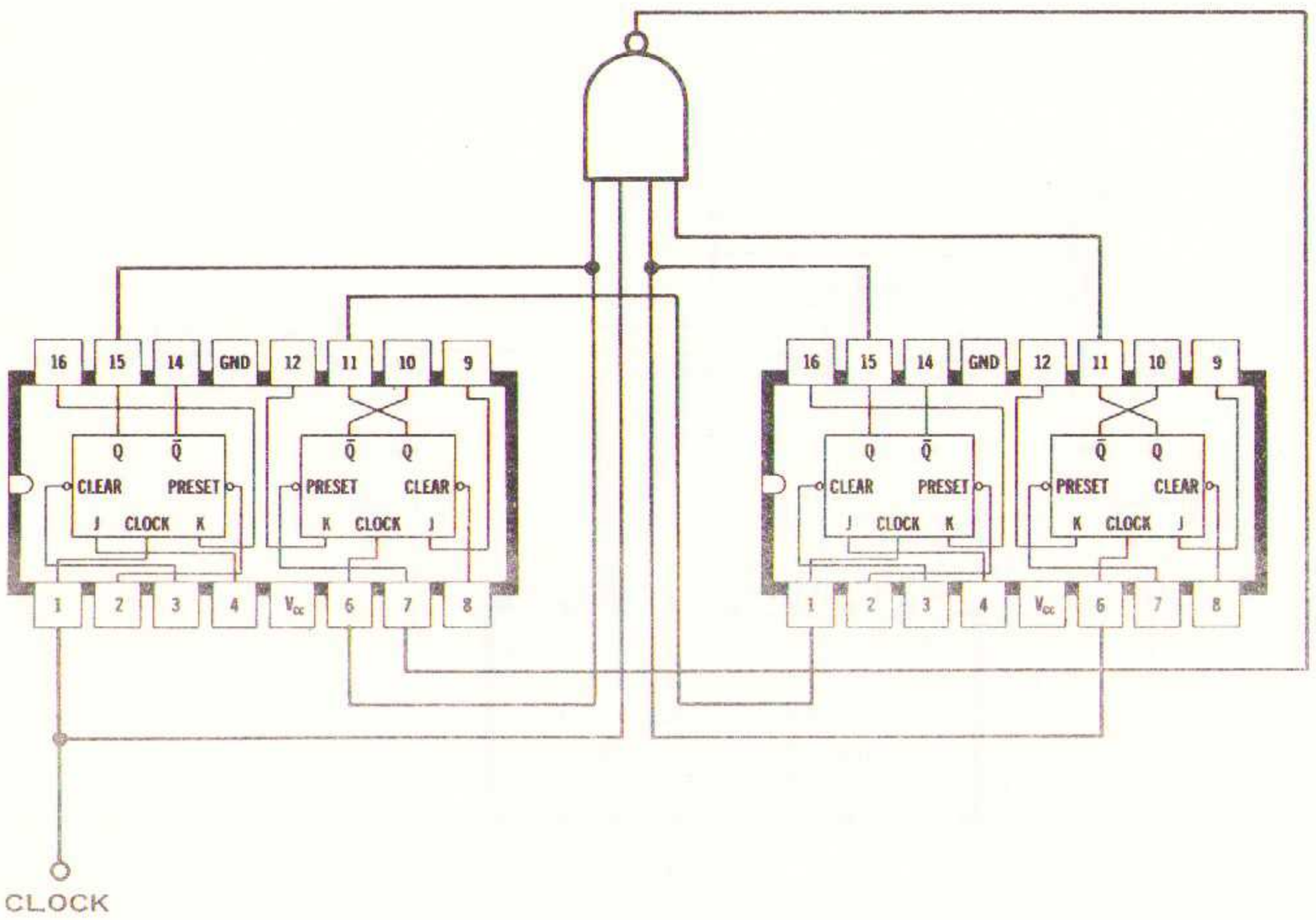


Figure 38. Divide-by-14 Binary Ripple Counter Using SN7476's

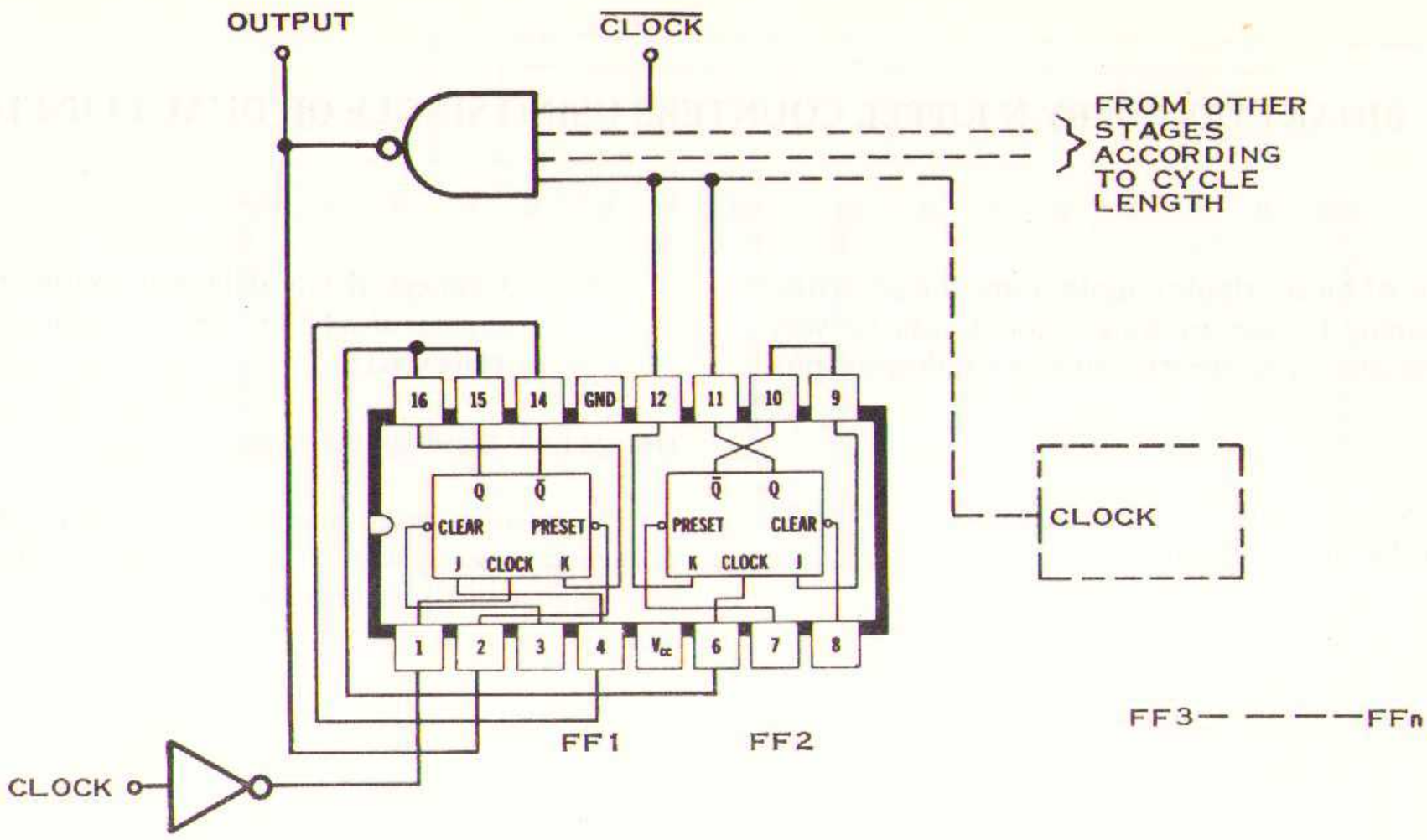


Figure 39. Divide-by-3 Binary Ripple Counter Using SN7476 With Delay Compensation

One restriction has to be made here. If the particular cycle length of the desired counter happens to require feedback from the NAND gate to the first stage, timing problems might be encountered. This can be eliminated by compensating for the delay of the NAND gate with an identical gate in the clock line. See Figure 39.

If $\overline{\text{clock}}$ is not available, the problem can be solved as shown in Figure 40.

This method is well suited for any length of count cycle. The maximum count frequency is a function of the total asynchronous propagation delay. For very long count cycles, the counter can be partitioned into a number of smaller counters which are operated in parallel with their outputs gated together.

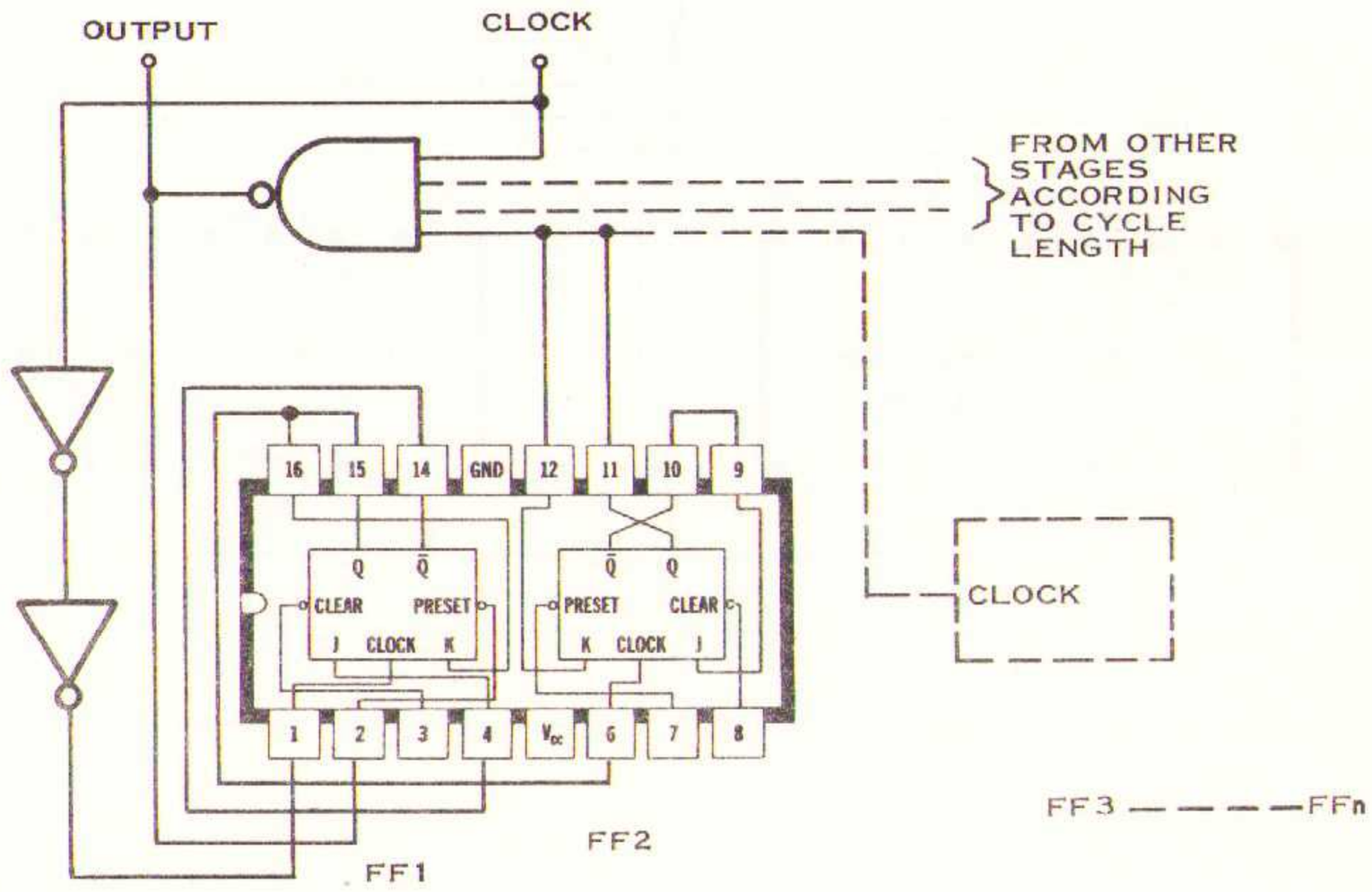


Figure 40. Divide-by-3 Binary Ripple Counter Using SN7476 When $\overline{\text{Clock}}$ Is Not Available

A very economical way to construct an asynchronous up/down counter is to use EXCLUSIVE-OR gates for the up/down control, as shown in Figure 40A.

The flip-flops used in this case have to be either master-slave type with data-lock-out or edge-triggered J-K or T types. When changing count direction, the synchronous inputs (J-K, T) are inhibited. Regular master-slave flip-flops of the type SN7472, -73, or -76 are not suited for this application because the data cannot be changed while the clock is high. Since some clock inputs are invariably high in an asynchronous counter while changing count direction, SN7472 master-slave flip-flops cannot be used in this application.

SN7474 edge-triggered D-type flip-flops modified to T type or the new series 54H100 series edge-triggered flip-flops can be used to build this triggered counter.

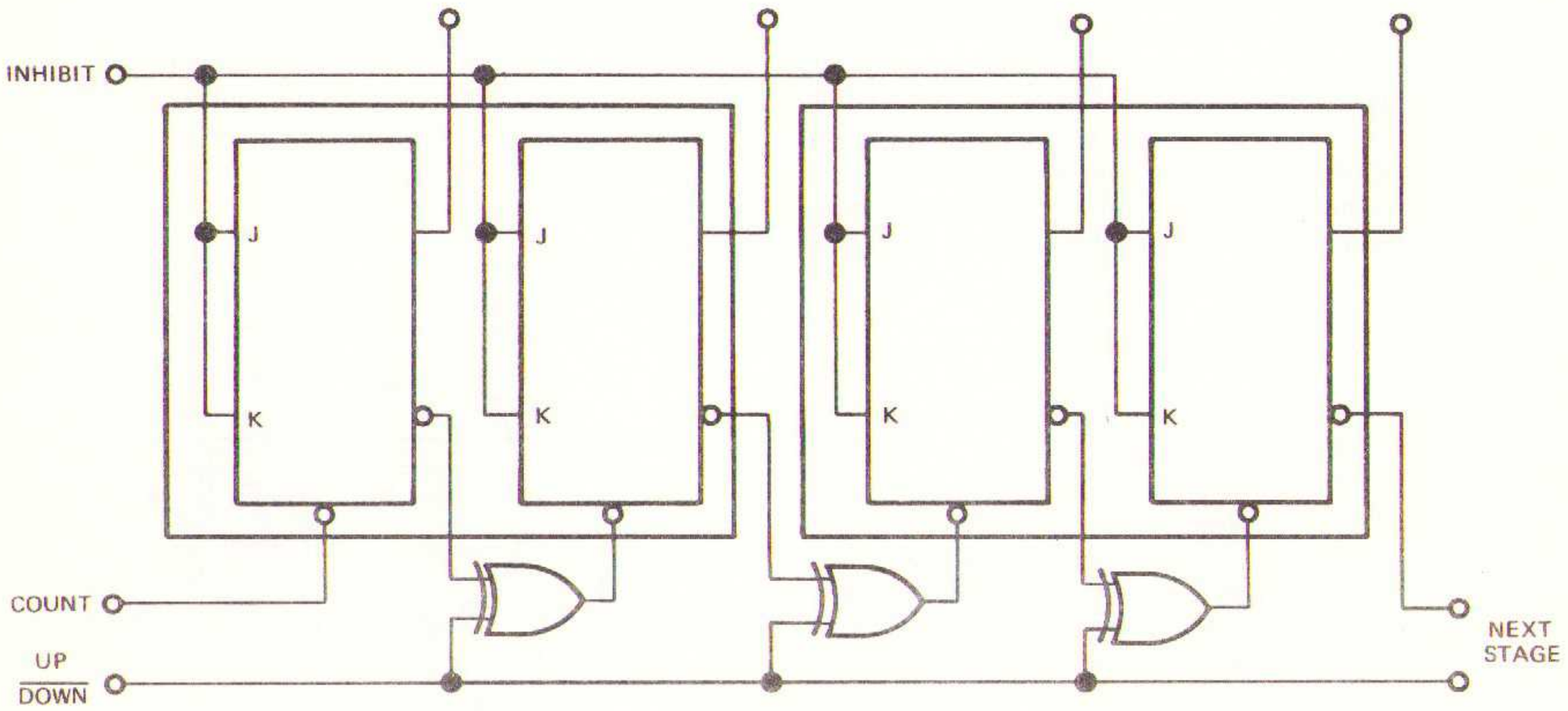


Figure 40A. 4-Bit Asynchronous Up/Down Ripple Counter

VIII. SYNCHRONOUS BINARY COUNTERS AND SHIFT COUNTERS

A. DESIGN PROCEDURE FOR SYNCHRONOUS COUNTERS

The advantage of synchronous counters is, that they can produce any binary sequence of any desired length without long delays for propagating the clock pulse. Since all memory elements change state at the same time (clock time), decoding spikes do not occur on the outputs. However, the number of components is usually larger than for other types of counters and the design procedure is more difficult if the cycle length is not a power of two.

For straight binary synchronous counters, for cycle lengths of 2, 2^1, 2^2, 2^3, 2^4, 2^5, ... 2^n, the design pattern can be seen in the following example illustrating a divide-by-13 synchronous counter. Note that the toggle or inhibit condition of a particular flip-flop (n) is a function of all previous flip-flops.

1. Divide-By-13 Synchronous Counter

   a. Write a state table for the desired code and cycle length (figure 41):

      (1) A transition map shows the actual sequence of states more clearly. See Figure 42. For codes other than the straight binary code more efficient state assignments can be found using common state assignment rules.

      (2) Next-State Karnaugh maps for flip-flop J and K input equations, figure 43.

Since each flip-flop has two inputs (J, K) and this counter requires four flip-flops (A, B, C, D), use eight 4-variable Karnaugh maps. If the transition map is considered as the present-state map, then the eight input maps can be considered next-state maps.

Example: From the state 0 1 1 1 (transition map) the counter goes to 1000. Since the J inputs set the flip-flops to Q = 1 (the K-inputs set the flip-flops to Q = 0), a "one" is entered in the A_J-map and "one" in the B_K, C_K, D_K maps (next state will be 1000).

      (3) Simplifying assumptions:

         (a) Only 13 out of 16 possible states are used – three "don't care" conditions exist. (X = unassigned states)

DECIMAL	PRESENT STATE				NEXT STATE			
	A	B	C	D	A	B	C	D
0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	0
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	1	0	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	1	0
6	0	1	1	0	0	1	1	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
10	1	0	1	0	1	0	1	1
11	1	0	1	1	1	1	0	0
12	1	1	0	0	0	0	0	0

Figure 41. State Table For Divide-by-13 Synchronous Counter

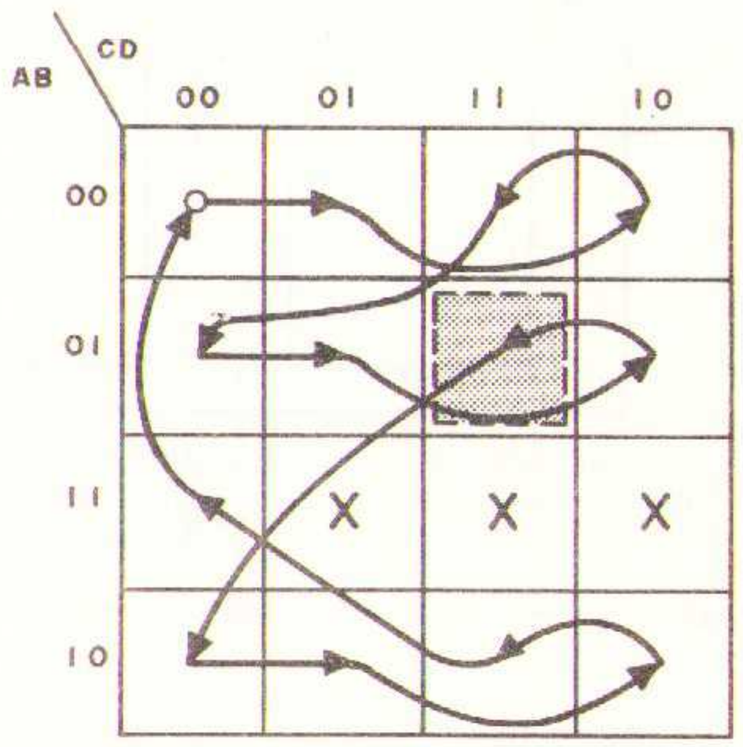


Figure 42. Transition Map For Divide-by-13 Synchronous Counter

   (b) For all conditions for which a "one" is entered in a map and the particular flip-flop is in the "one" state already a no-change ("don't care") can be used to simplify.

Φ = no change

Since a J-K flip-flop changes state for J-K = 1 a "one" in the J-Maps can be plotted as a toggle "don't care" (Φ) in the K-maps.

Φ = Toggle

b. With these simplifications, the input equations to the four flip-flops can be solved from the J-K input next-state maps:

$A_J = BCD$

$A_K = B$

$B_J = CD$

$B_K = CD+A$

$C_J = D$

$C_K = D$

$D_J = \overline{A} + \overline{B} = \overline{A\,B}$

$C_K = 1$

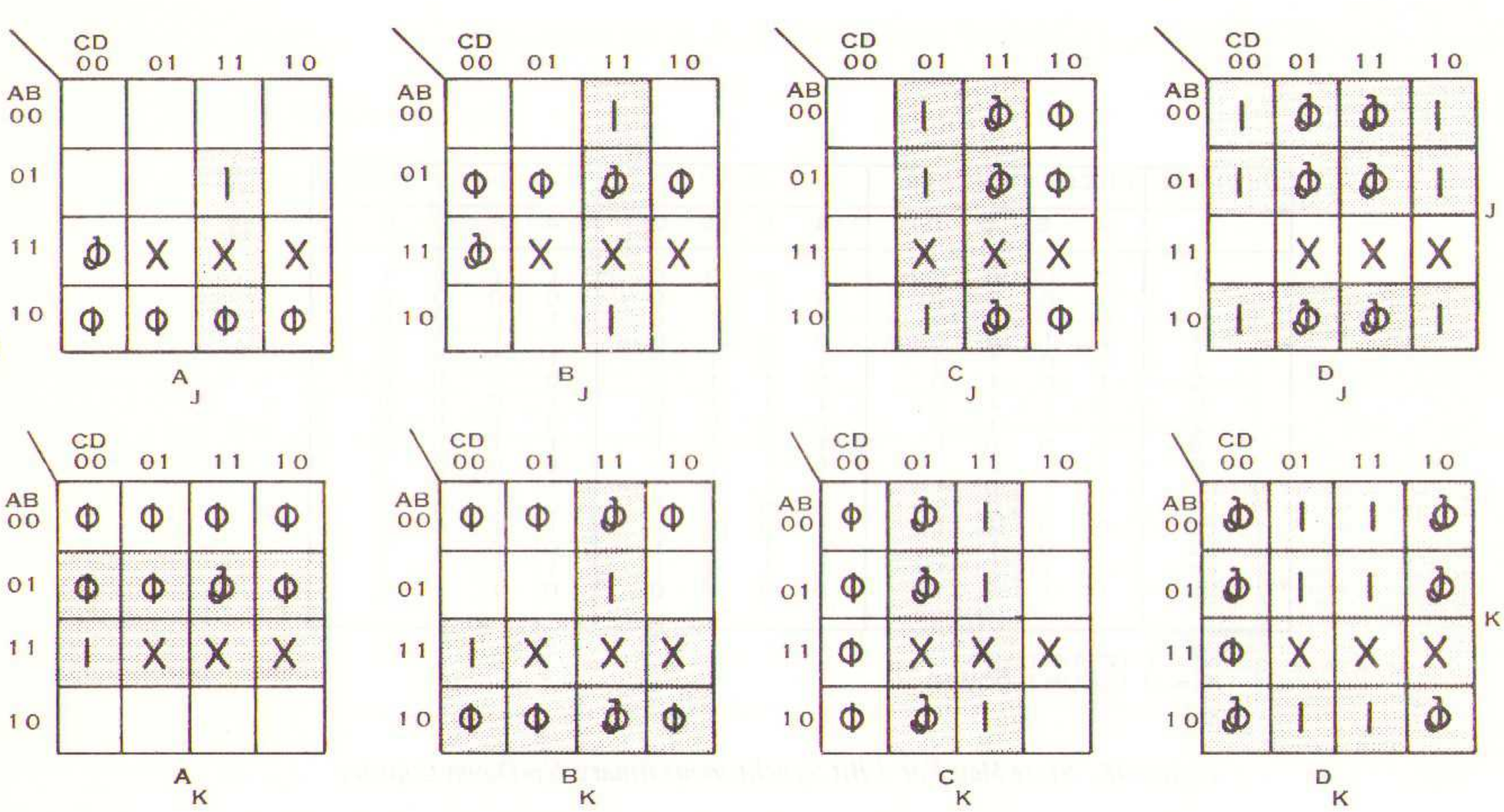


Figure 43. J and K Input Next-State Maps For Divide-by-13 Synchronous Counter

c. Logic Implementation of Divide-By-13 Synchronous Counter is shown in Figure 44.

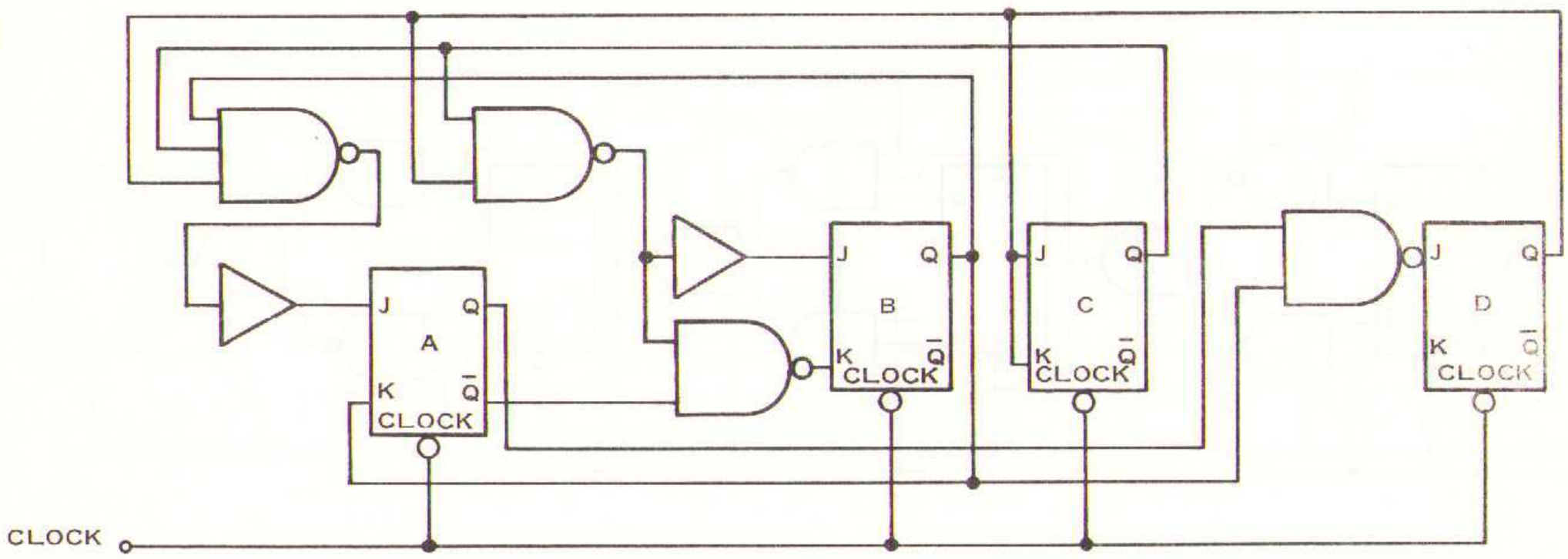


Figure 44. Divide-by-13 Synchronous Counter

2. 4-Bit Binary - UP-DOWN Counter:

a. Transition Table (Figure 45):

b. Logic Implementation of 4-Bit Binary Synchronous Counter

There are two different arrangements shown which represent a trade-off between speed and hardware especially for long cycle lengths.

(1) Serial-Carry method (Figure 46)

(2) Parallel-Carry method (Figure 47)

DECIMAL	PRESENT STATE				X = 1				X = 0			
	A	B	C	D	A	B	C	D	A	B	C	D
0	0	0	0	0	1	0	0	0	1	1	1	1
1	1	0	0	0	0	1	0	0	0	0	0	0
2	0	1	0	0	1	1	0	0	1	0	0	0
3	1	1	0	0	0	0	1	0	0	1	0	0
4	0	0	1	0	1	0	1	0	1	1	0	0
5	1	0	1	0	0	1	1	0	0	0	1	0
6	0	1	1	0	1	1	1	0	1	0	1	0
7	1	1	1	0	0	0	0	1	0	1	1	0
8	0	0	0	1	1	0	0	1	1	1	1	0
9	1	0	0	1	0	1	0	1	0	0	0	1
10	0	1	0	1	1	1	0	1	1	0	0	1
11	1	1	0	1	0	0	1	1	0	1	0	1
12	0	0	1	1	1	0	1	1	1	1	0	1
13	1	0	1	1	0	1	1	1	0	0	1	1
14	0	1	1	1	1	1	1	1	1	0	1	1
15	1	1	1	1	0	0	0	0	0	1	1	1

X = 1 (COUNT UP)
X = 0 (COUNT DOWN)

Figure 45. State Map For 4-Bit Synchronous Binary Up-Down Counter

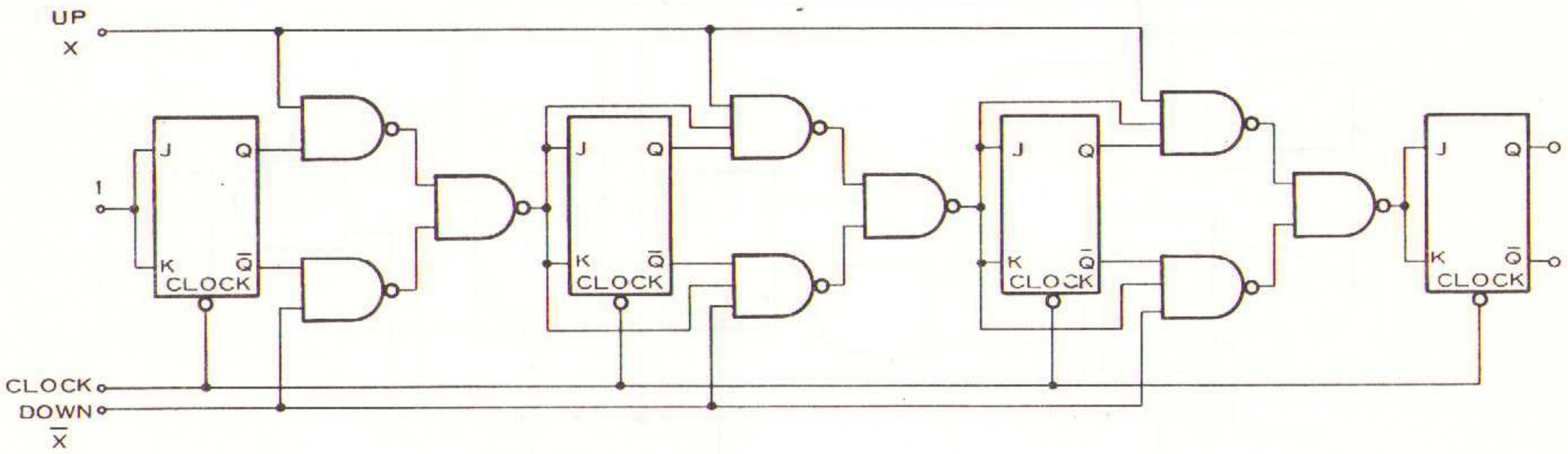


Figure 46. 4-Bit Synchronous Binary Up-Down Counter (Serial Carry) Using SN7473's

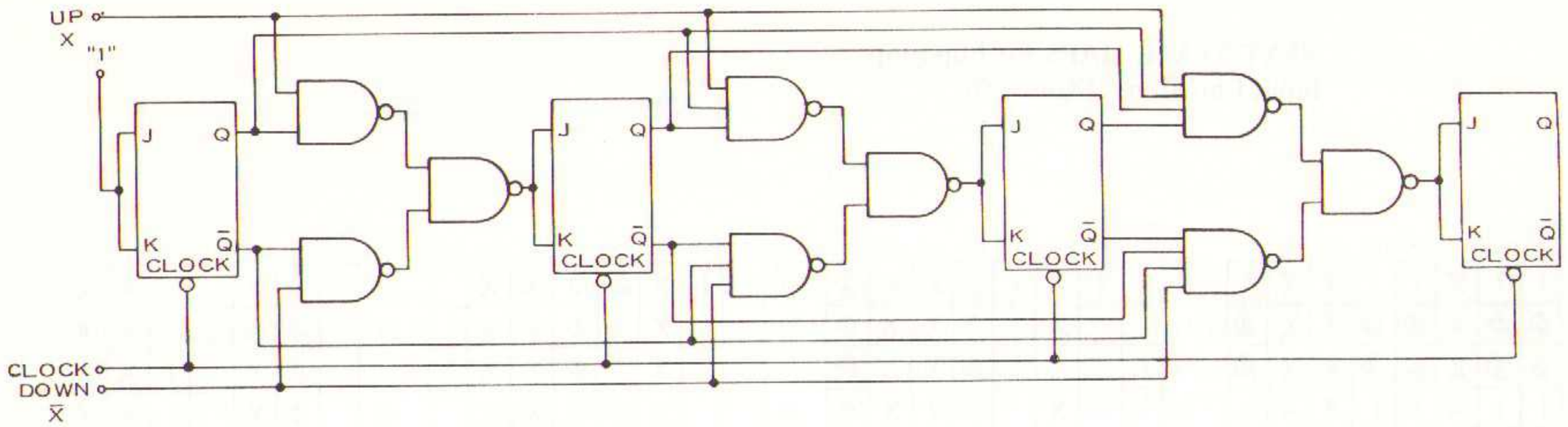


Figure 47. 4-Bit Synchronous Binary Up-Down Counter (Parallel Carry) Using SN7473's

3. Up-Down Decade Counter:

a. State-diagram (Figure 48):

(1) Transition Map (Figure 49)

DEC.	PRESENT STATE				NEXT STATES X = 1				X = 0			
	D	C	B	A	D	C	B	A	D	C	B	A
0	0	0	0	0	0	0	0	1	1	0	0	1
1	0	0	0	1	0	0	1	0	0	0	0	0
2	0	0	1	0	0	0	1	1	0	0	0	1
3	0	0	1	1	0	1	0	0	0	0	1	0
4	0	1	0	0	0	1	0	1	0	0	1	1
5	0	1	0	1	0	1	1	0	0	1	0	0
6	0	1	1	0	0	1	1	1	0	1	0	1
7	0	1	1	1	1	0	0	0	0	1	1	0
8	1	0	0	0	1	0	0	1	0	1	1	1
9	1	0	0	1	0	0	0	0	1	0	0	0

X = 1 (COUNT UP)
X = 0 (COUNT DOWN)

Figure 48. State Map For Synchronous Up-Down Decade Counter

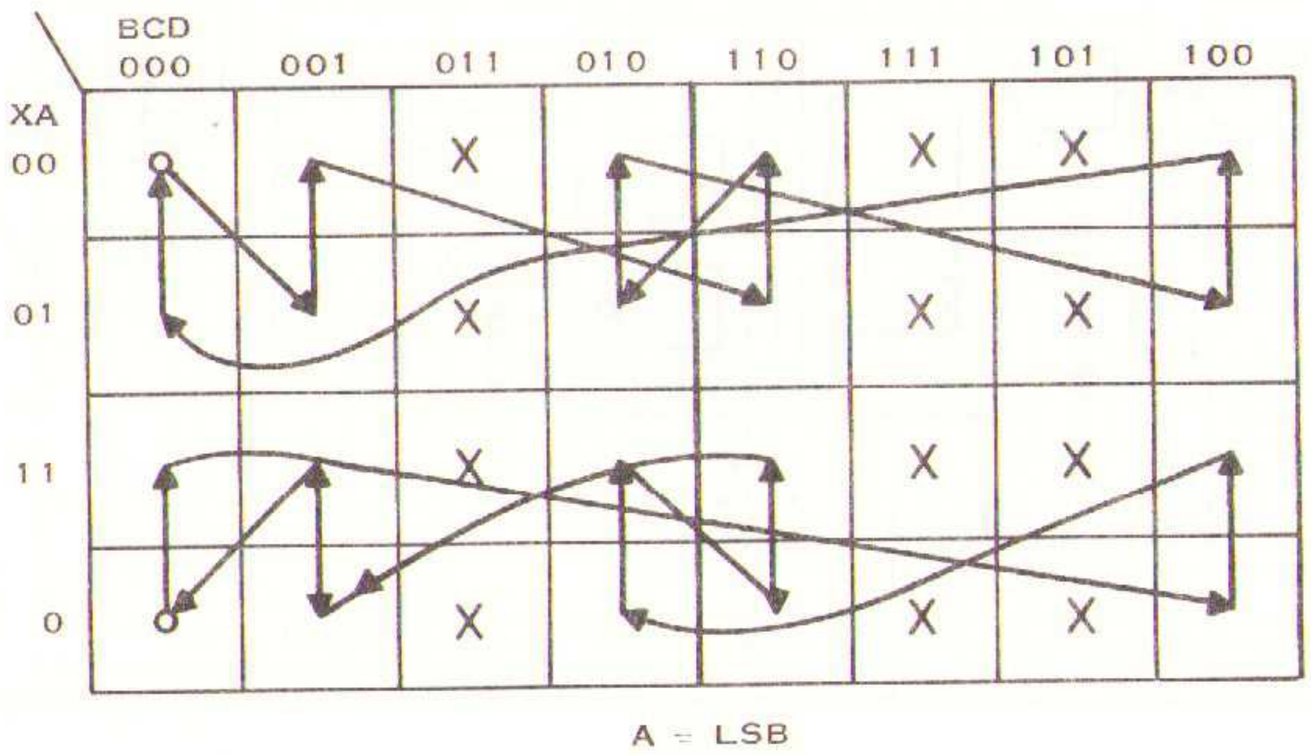


Figure 49. Transition Map For Synchronous Up-Down Decade Counter

(2) NEXT STATE MAPS for Flip-Flop Input Equations (Figure 50):

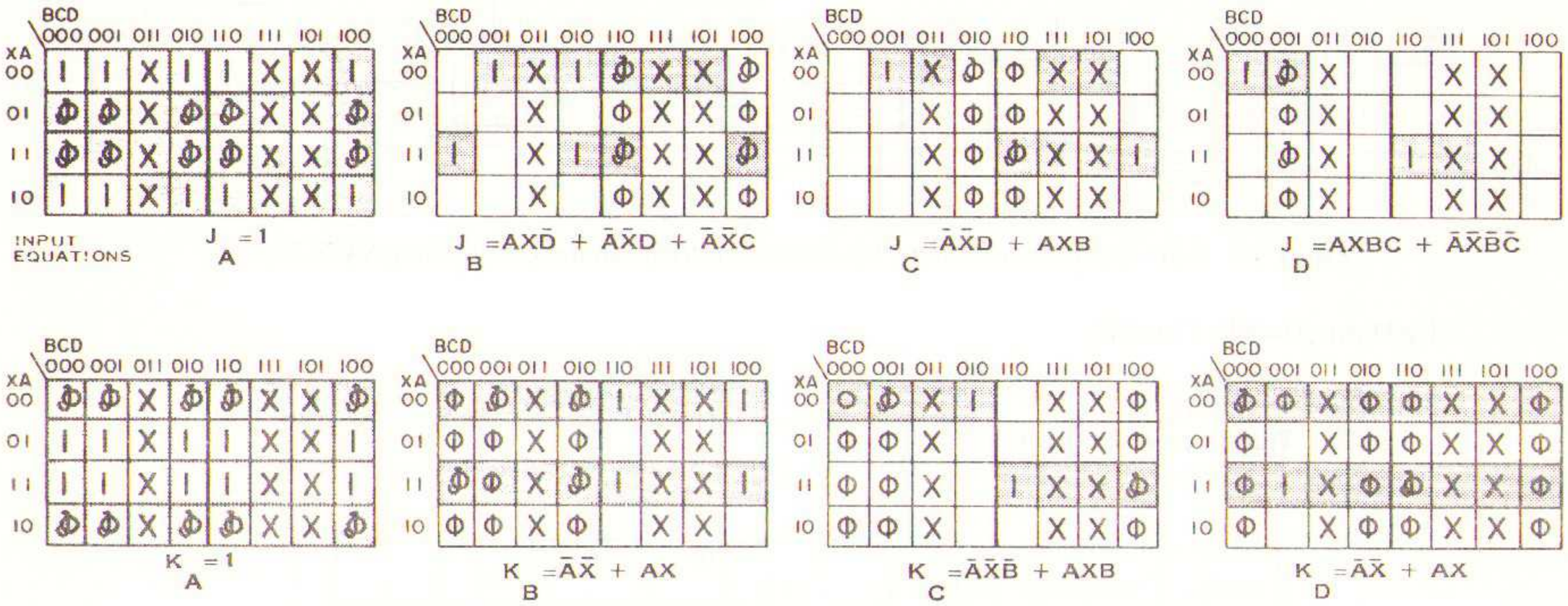


Figure 50. Next-State Maps For Synchronous Up-Down Decade Counter

b. Logic Implementation of Synchronous Up-Down Decade Counter (Figure 51)

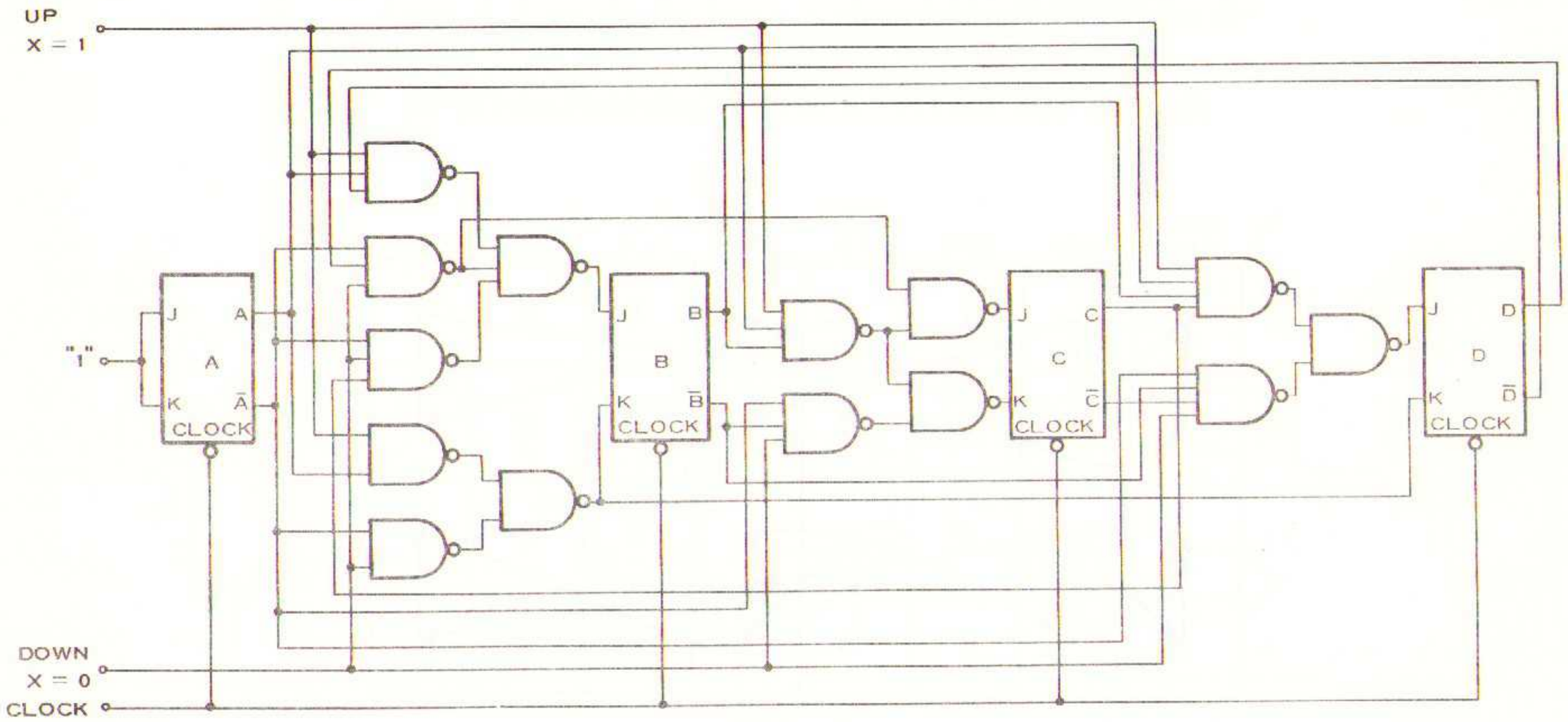


Figure 51. Synchronous Up-Down Decade Counter

B. BINARY UP-DOWN SYNCHRONOUS COUNTER USING THE SN7474 DUAL D-TYPE FLIP-FLOPS

Counting can be considered as repeated addition of 1 to the contents of a register.

EXAMPLE:

The number held in a register is 13 (binary 1 1 0 1)

Add 1	1 1 0 1
Add 1	+0 0 0 1
Gives 14	1 1 1 0
13	1 1 0 1
Subtract 1	-0 0 0 1
Gives 12	1 1 0 0

The same result is achieved by adding the 2's complement of 1 to 13, instead of subtracting 1.

13	1 1 0 1
Add 2's complement of 1	+1 1 1 1
	1.1 1 0 0
	1 1 0 0

This result is $12_{(10)}$ with a carry which may be considered as a sign bit.

EXAMPLE:

The maximum frequency is determined by the propagation delay of the serial carry in the adder. For eight stages, the frequency is still above 10 MHz, when considering 70 ns carry propagation delay for two SN7483's plus 15 ns(typical) set-up time for the SN7474.

$$tp = 70 + 15 = 85 \text{ ns}$$

$$f = \frac{1}{tp} = \frac{1}{85} \bullet 10^9 \approx 12 \text{ MHz}$$

These counters are very useful as incrementer and program counters.

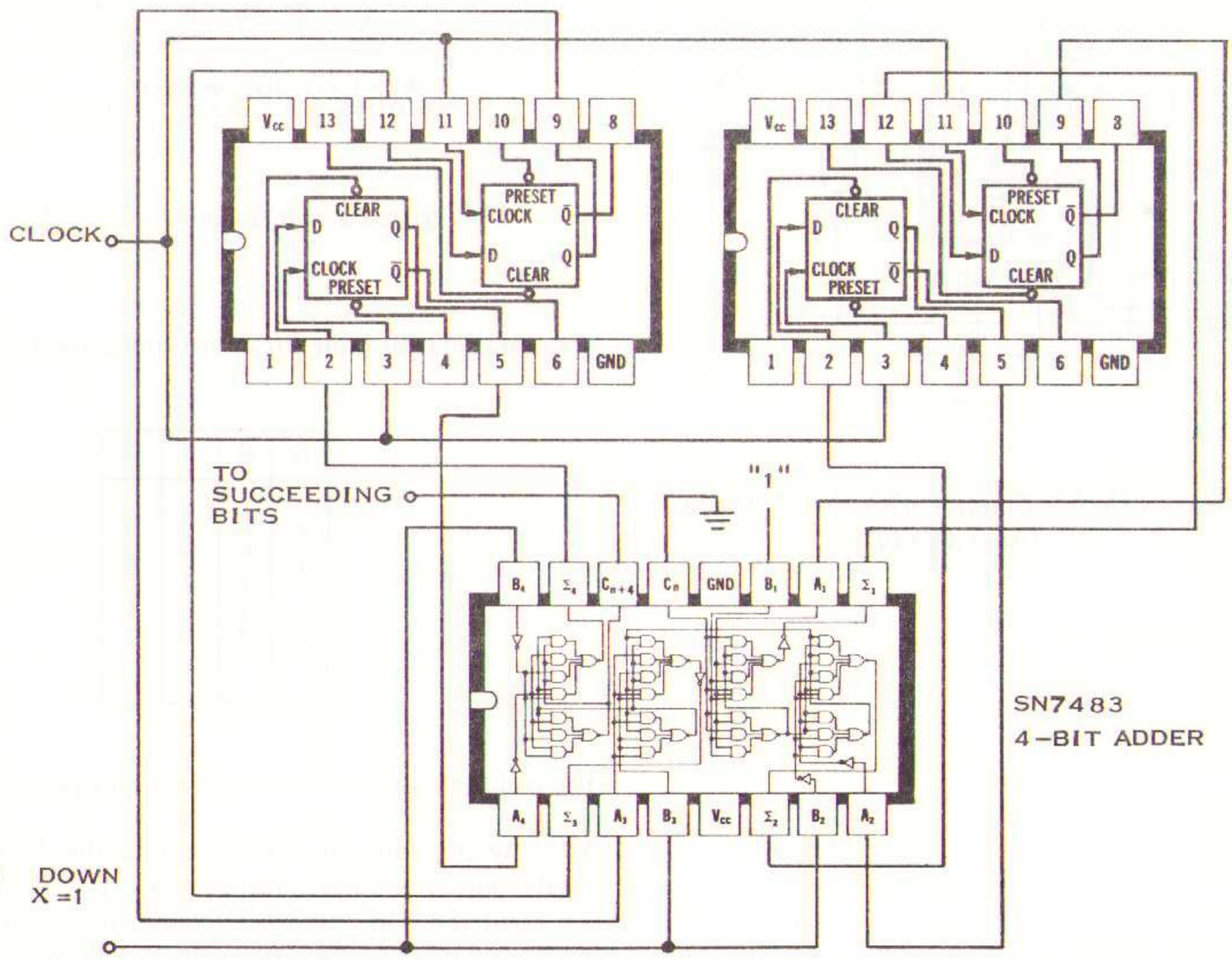


Figure 52. Binary Up-Down Synchronous Counter Using SN7474 Flip-Flops

IX. SHIFT-COUNTERS USING SN7495

In applications where all outputs of a counter need to be decoded, an SN7495 shift register used as a shift counter and two SN7442 three-to-eight or four-to-ten-line decoders can perform the function of an up/down decade counter with all outputs decoded. An example is shown in Figure 52A.

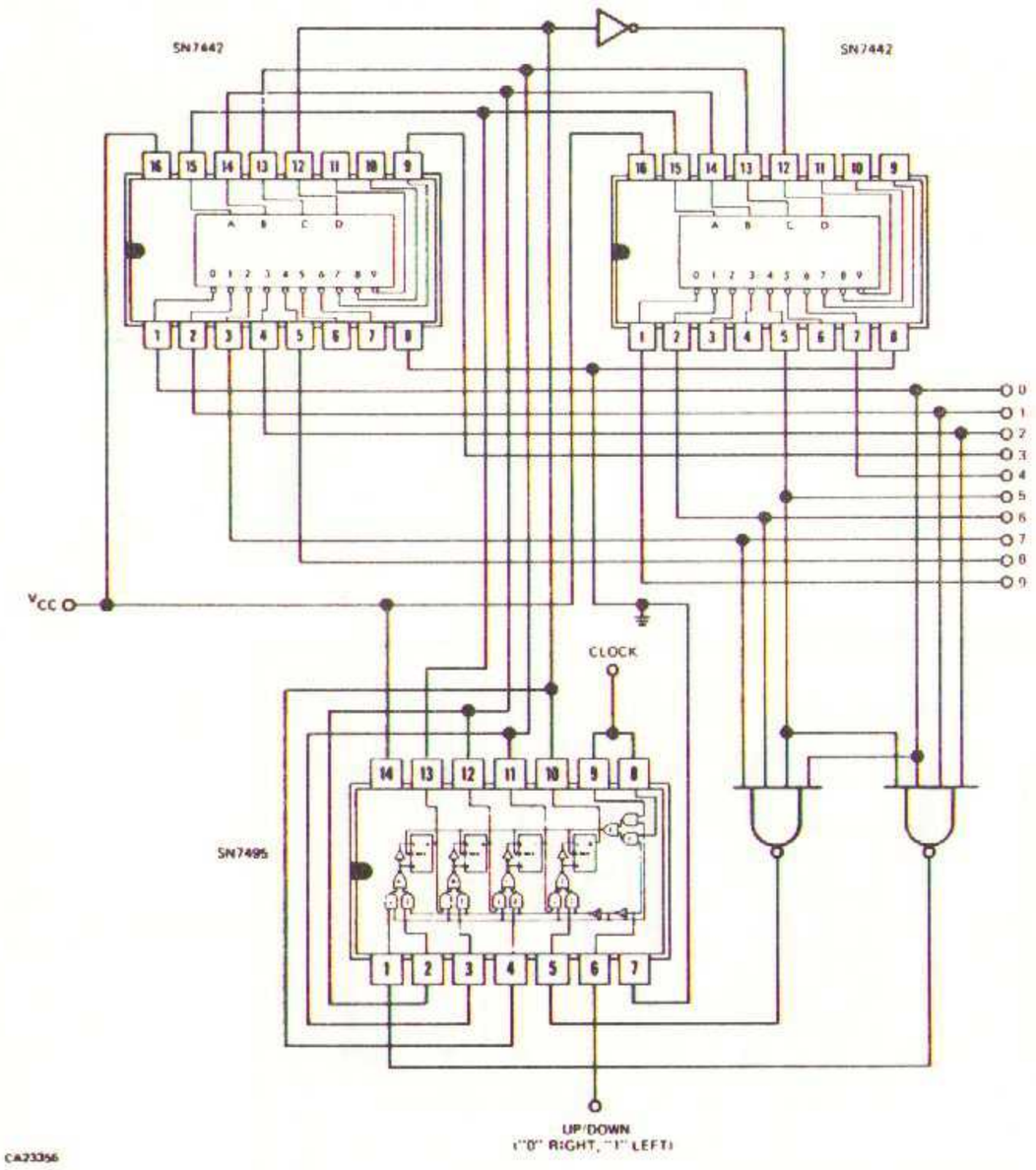


Figure 52A. Up/Down Decade Counter With Decode Outputs Using SN7495

The SN7495 can be programmed as a shift counter by applying a feedback circuit from the outputs to "mode control". When the parallel inputs are tied to a binary word according to Figure 54, then the counter recycles according to the inputs fed into the NAND gate:

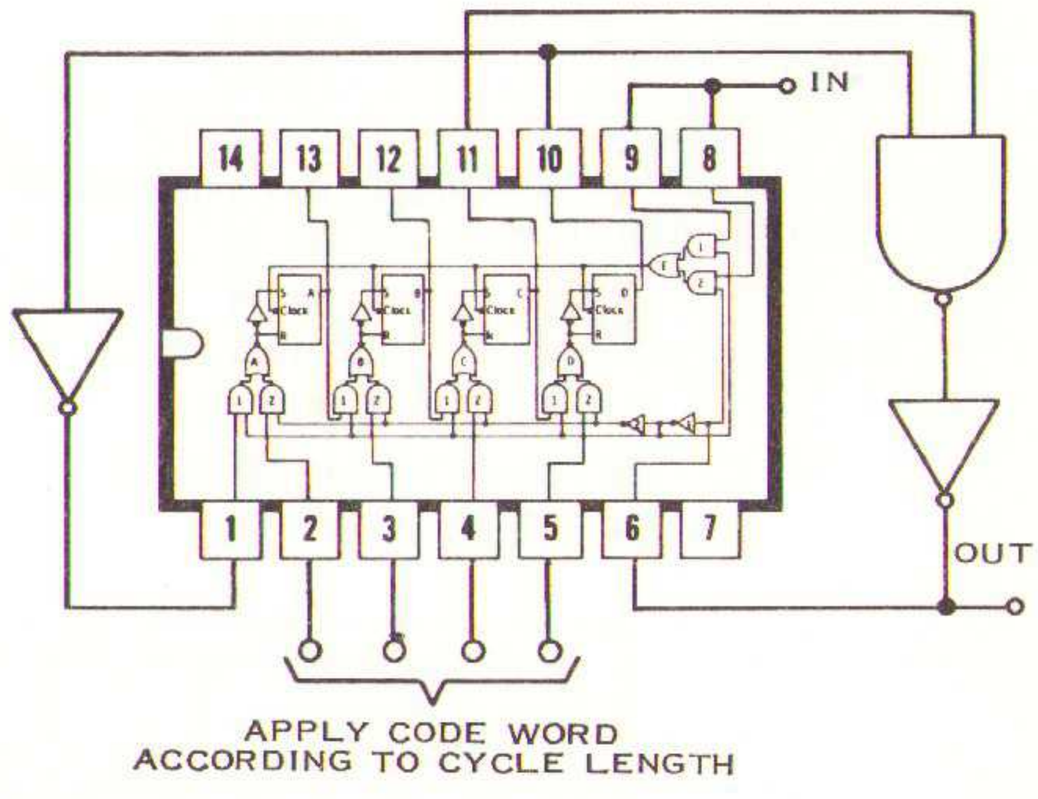


Figure 53. Shift-Counter Using SN7495

Example: Truth table for above configuration:

A	B	C	D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
0	0	1	0

The counter recycles for every five input pulses.

Also, by providing feedback around the SN7495 to the serial input, cycle lengths from two to eight can be achieved. See Figure 54. One necessary condition is that the counter must be set to a known state at the beginning of the cycle or if it mistriggers to a state which is not part of the count. This can be achieved with the SN7495 by setting the parallel inputs to the recycle state and strobing the mode control. This will set the register in the first state of the count cycle.

DIVIDE–BY–2 STATE OF OUTPUTS				FEEDBACK TERM	DIVIDE–BY–3 STATE OF OUTPUTS				FEEDBACK TERM
Q_A	Q_B	Q_C	Q_D	$\overline{Q}_A$	Q_A	Q_B	Q_C	Q_D	$\overline{Q_A Q_B}$
0	1	0	0	1	1	1	0	0	0
1	0	1	0	0	0	1	1	0	1
0	1	0	1	1	1	0	1	1	1
1	0	1	0	0	1	1	0	1	0
0	1	0	1	1	0	1	1	0	1
					1	0	1	1	1
					1	1	0	1	0

DIVIDE–BY–4 STATE OF OUTPUTS				FEEDBACK TERM	DIVIDE–BY–5 STATE OF OUTPUTS				FEEDBACK TERM
Q_A	Q_B	Q_C	Q_D	$\overline{Q}_B$	Q_A	Q_B	Q_C	Q_D	$\overline{Q_B Q_C}$
1	1	0	0	0	1	1	0	0	1
0	1	1	0	0	1	1	1	0	0
0	0	1	1	1	0	1	1	1	1
1	0	0	1	1	0	0	1	1	1
1	1	0	0	0	1	0	0	1	0
0	1	1	0	0	1	1	0	0	0
0	0	1	1	1	1	1	1	0	1
1	0	0	1	1	0	1	1	1	1
1	1	0	0	0	0	0	1	1	0
1	1	1	0	0	1	0	0	1	0
0	1	1	1	0	0	1	0	0	1

DIVIDE–BY–6 STATE OF OUTPUTS				FEEDBACK TERM	DIVIDE–BY–7 STATE OF OUTPUTS				FEEDBACK TERM
Q_A	Q_B	Q_C	Q_D	$\overline{Q}_C$	Q_A	Q_B	Q_C	Q_D	$\overline{Q_C Q_D}$
1	0	0	0	1	1	0	0	0	1
1	1	0	0	1	1	1	0	0	1
1	1	1	0	0	1	1	1	0	1
0	1	1	1	0	1	1	1	1	0
0	0	1	1	0	0	1	1	1	0
0	0	0	1	1	0	0	1	1	0
1	0	0	0	1	0	0	0	1	1
1	1	0	0	1	1	0	0	0	1
1	1	1	0	0					
0	1	1	1	0					

DIVIDE–BY–8 STATE OF OUTPUTS				FEEDBACK TERM
Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
1	0	0	0	1
1	1	0	0	1
1	1	1	0	1
1	1	1	1	0
0	1	1	1	0
0	0	1	1	0
0	0	0	1	0
0	0	0	0	1
1	0	0	0	1

Figure 54. Variations of SN7495 Shift-Counter Cycle-Length

X. JOHNSON COUNTERS

JOHNSON COUNTERS FOR EVEN- AND ODD-CYCLE LENGTHS USING THE SN7472, SN7473, SN7491, SN7494, SN7496

These registers can be used to build another counter type. The counters to be discussed here are shift-register counters and are called Johnson Counters. These counters work synchronously and can be operated at typically 25 MHz using the SN7400 series. They can be very easily designed and the output decoding is very simple, especially where several counts need to be decoded. Successive division ratios of 2, 4, 6, 8, 10 can be taken from the outputs, if the E output is inverted and fed back to the input. See Figure 55.

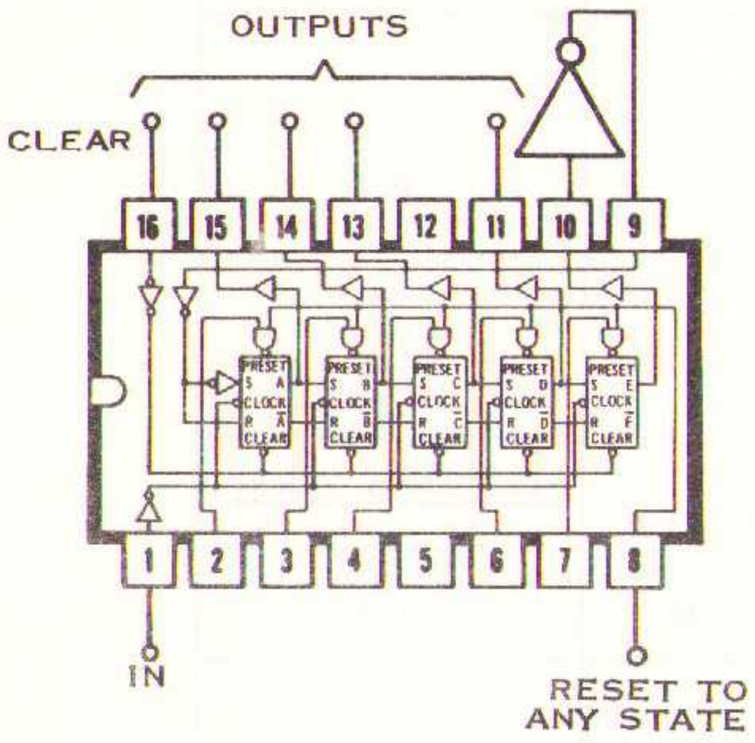


Figure 55. Johnson Counter For Even-Cycle Length Using SN7496

For odd-cycle length, add gating to skip the all "1" state by feeding a "0" in the first stage:

```
1  1  1  1  0  –  DETECT THIS STATE
1  1  1  1  1  –  SKIP THIS STATE
0  1  1  1  1  –  GO DIRECTLY TO THIS STATE
```

Division ratios of 3, 5, 7, 9 in the Johnson cycle can be taken from the outputs of the SN7496. See Figure 56.

The cycle length of the Johnson counter is $2 \cdot n$ instead of 2^n. Therefore, more flip-flops are required for a given cycle length. On the other hand, a unique pattern is generated which allows any count to be decoded with a simple 2-input NAND gate. See Figure 57.

If asynchronous inputs (preset and clear) can be used to set the counter in a known state when it jumps out of the cycle or at the beginning of a count, the SN7491, SN7494, SN7496 may be used. Otherwise, gating must be provided to ensure that it will enter the correct cycle and count back into this cycle if it jumps out.

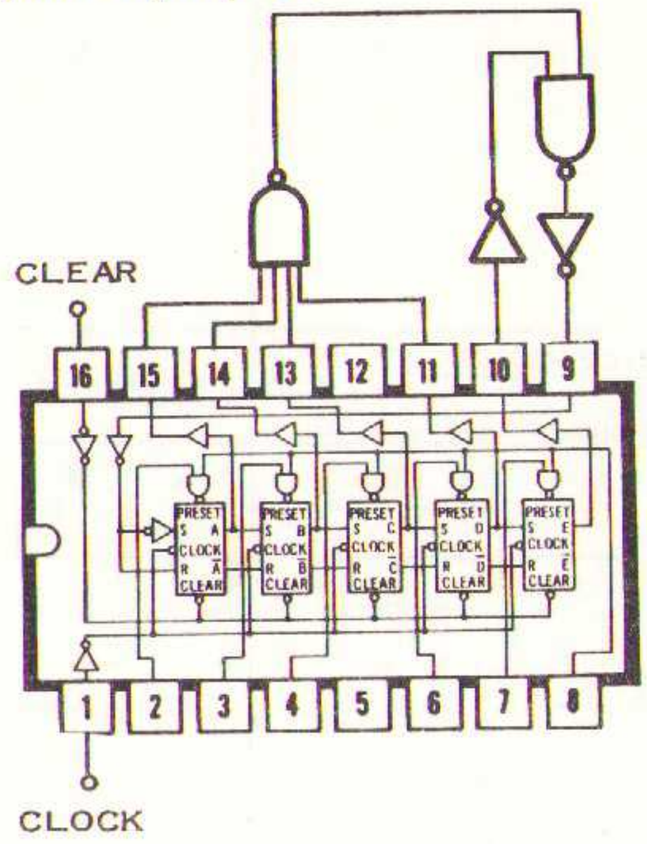


Figure 56. Johnsön Counter For Odd-Cycle Length Using SN7496

DECIMAL	A	B	C	D	E	OUTPUT DECODING
0	0	0	0	0	0	$\bar{A}$ $\bar{E}$
1	1	0	0	0	0	A $\bar{B}$
2	1	1	0	0	0	B $\bar{C}$
3	1	1	1	0	0	C $\bar{D}$
4	1	1	1	1	0	D $\bar{E}$
5	1	1	1	1	1	A $\bar{E}$
6	0	1	1	1	1	$\bar{A}$ B
7	0	0	1	1	1	$\bar{B}$ C
8	0	0	0	1	1	$\bar{C}$ D
9	0	0	0	0	1	$\bar{D}$ E

Figure 57. Truth Table For Even-Cycle Length SN7496 Johnson Counter

The Johnson cycle is not self-starting without additional feedback. It has been found that the Johnson cycle is always self-starting (for n up to 25 stages) when feedback is provided from the last j stages of an n-stage shift register, where

$$j > \frac{n}{3}$$

Six-stage self-starting Johnson counters are illustrated in Figures 58 and 59. These counters can also be implemented using SN7474 dual flip-flops.

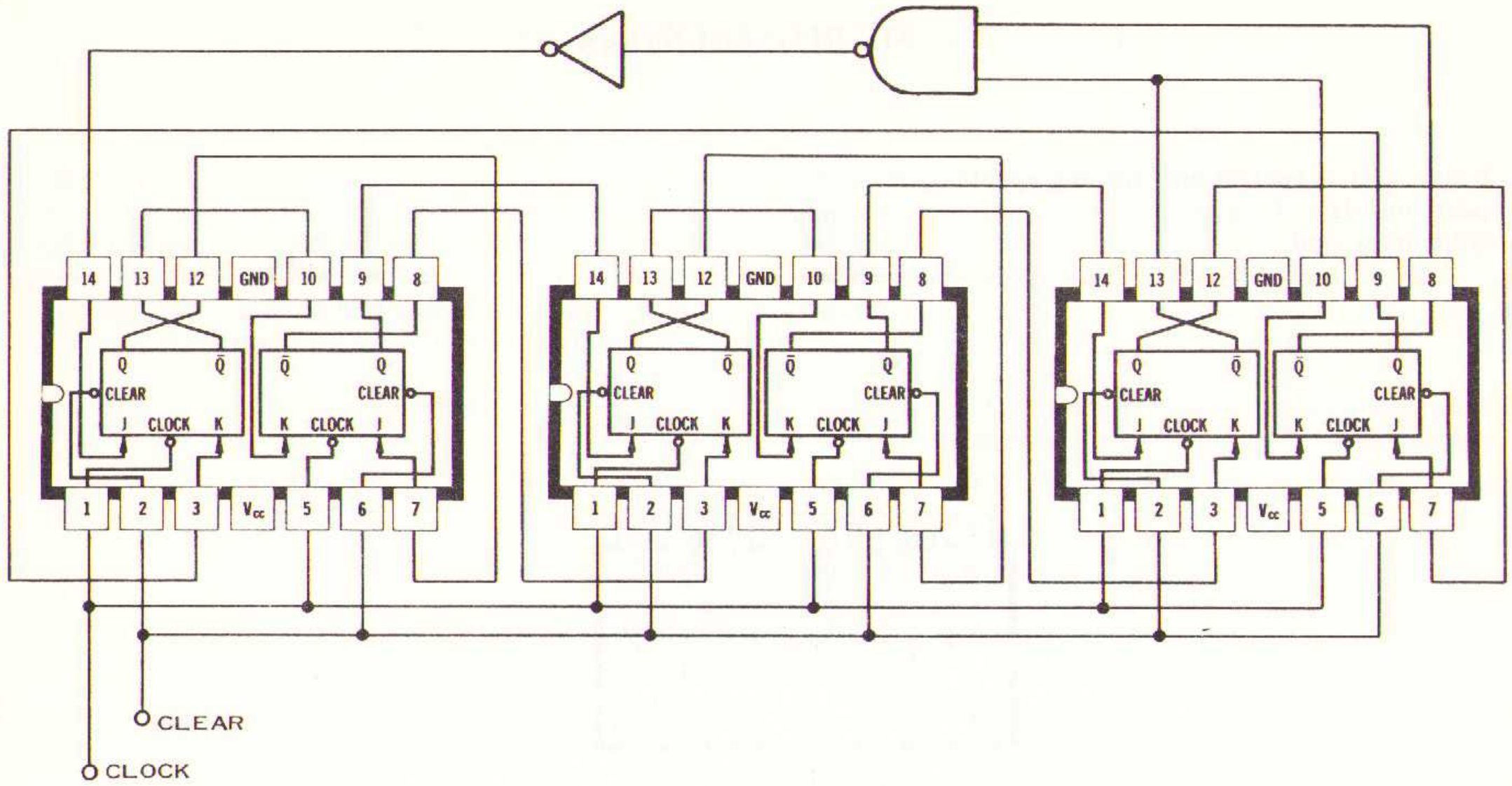


Figure 58. Self-Starting Six-Stage, Even-Cycle Length Johnson Counter Using SN7493's

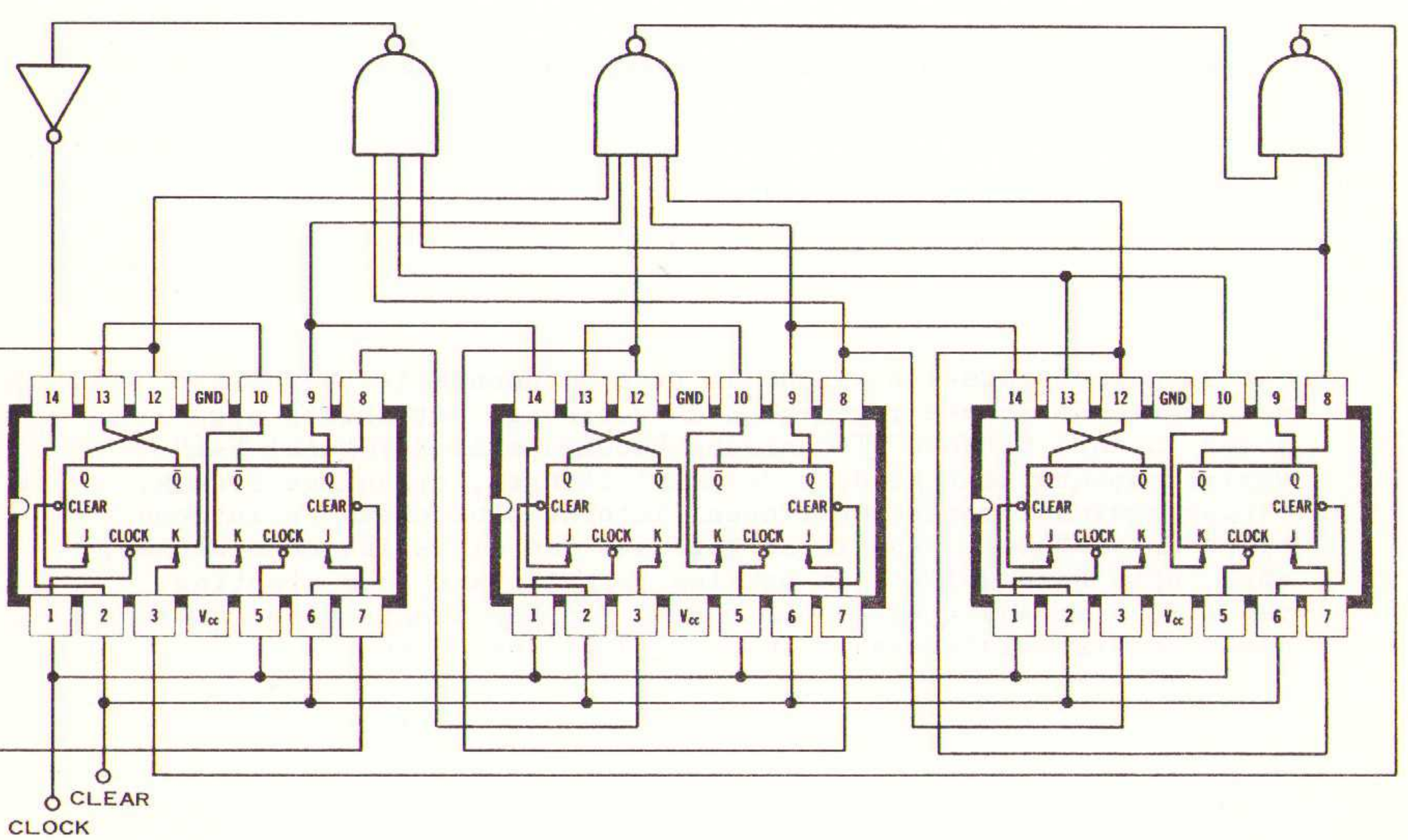


Figure 59. Self-Starting Six-Stage, Odd-Cycle Length Johnson Counter Using SN7493's

XI. RING COUNTERS

Ring counters contain only one logical "1" or "0" and circulate this data. Total cycle length is equal to their number of flip-flops used.

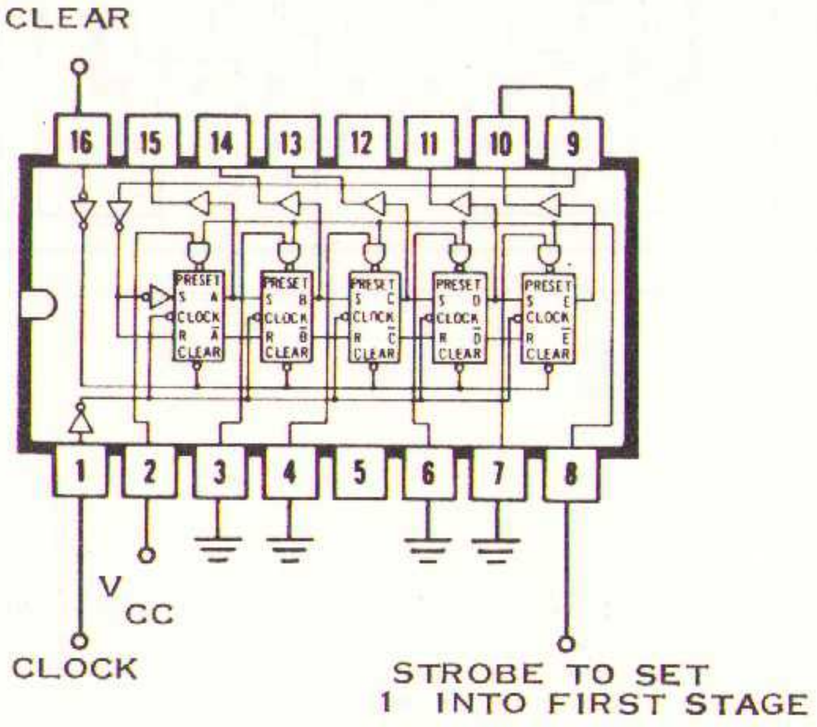


Figure 60. Divide-by-5 Ring Counter Using SN7496

XII. SHIFT REGISTER GENERATOR COUNTERS

Other types of counters which can be built easier than synchronous binary counters and which becomes very economical for large cycle lengths are called linear shift register generator counters. These counters are shift register counters which use a mod. 2 feedback. These counters are synchronous counters and are divided into two classes:

(1) Maximum length counters

(2) Non-maximum length counters

A. MAXIMUM LENGTH COUNTERS

Maximum length counters count to a cycle length of 2^n-1 (with n = number of stages in the shift register).

An exclusive–OR feedback term is provided from an even number of stages to the first stages. The stages to be fed back can be found in Table I for up to 12 stages.

Table I. Feedback Connections For Maximum-Length Linear Shift Register Generator Counters (MLS)

NUMBER OF STAGES IN THE SHIFT REGISTER	FEEDBACK STAGES											
	A	B	C	D	E	F	G	H	I	J	K	L
3	0	1	1									
4	0	0	1	1								
5	0	0	1	0	1							
6	0	0	0	0	1	1						
7	0	0	0	0	0	1	1					
8	0	0	0	1	1	1	0	1				
9	0	0	0	0	1	0	0	0	1			
10	0	0	0	0	0	0	1	0	0	1		
11	0	0	0	0	0	0	0	0	1	0	1	
12	0	0	0	0	0	1	0	1	0	0	1	1

Note: The feedback equation is the modulo 2 sum of the "1" terms in Table I.

Since the modulo 2 sum of two zeros is zero, the all zero states of the register have to be excluded from the counting sequence. This can be achieved by either additional gating or with the asynchronous preset inputs.

Example:

Use SN7496 to count to 31. The feedback term from above table for 5 stages is:

$$F = C\overline{E} + \overline{C}\,\overline{E}$$

Another method of inhibiting the all zero state is to add the AND term of all zero outputs ($\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E}$) to the feedback equation:

$$F = C\overline{E} + \overline{C}E + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D}\ \overline{E}$$

which simplifies to:

$$F = C\overline{E} + \overline{C}E + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D}$$

See Figure 61.

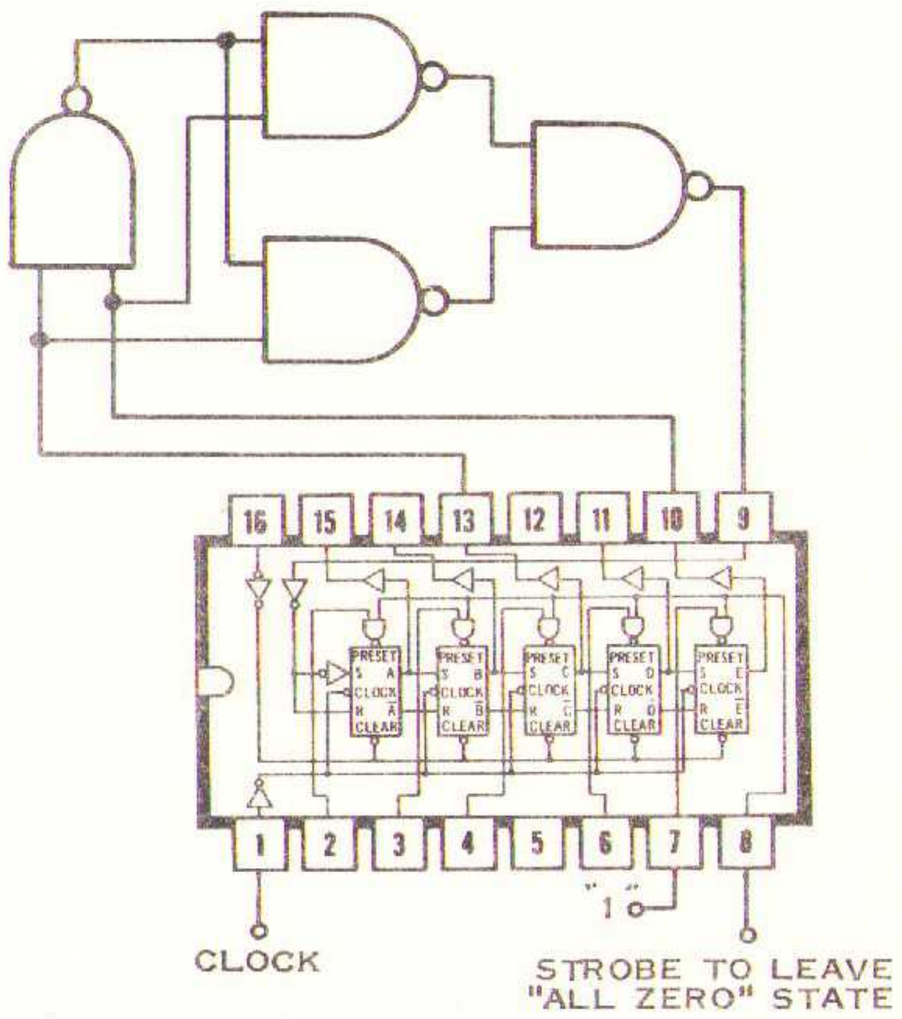


Figure 61. Divide-by-31 Shift-Register Generator Counter Using SN7496

Another modification allows a count to 2^n instead of $2^n - 1$ (for n stages).

By adding a term to the feedback equation which inhibits the feedback (zero output of all stages, except the last, and the one output of the last stage ($\overline{A}\ \overline{B}\ \overline{C}\ \overline{D}\ E$), the counter can be forced into the all zero state. At the next clock pulse the counter leaves the all zero state again on account of the term previously added.

Feedback equation for cycle length 2^n for n = 5:

$$F = (C\overline{E} + \overline{C}E) \cdot \overline{(\overline{A}\ \overline{B}\ \overline{C}\ \overline{D}\ E)} + \overline{A}\ \overline{B}\ \overline{C}\ \overline{D}\ \overline{E}$$

These counters can also be built with the SN7473, SN7474, SN7476, SN7494, SN7495.

B. NON-MAXIMUM LENGTH COUNTERS

Here a technique referred to as the "jump technique" is described to shorten the cycle described above. Basically, another term is added to the technique described under (1) which forces, at a certain state, a 0 or 1 into the first stage, when a "1" or "0" is dictated by the mod. 2 feedback. Effectively, the counter jumps over a determined number of stages (k) for $K < 2^n - 1$. Therefore, any desired cycle length can be generated.

Example:

Use the SN7496 to divide by 21. The maximum length cycle is $2^5 - 1 = 31$ (31-21 = 10) 10 stages must be jumped.

The design is the same as for MLS except that a jump term must be added to the feedback equation. See Figure 62.

Table I indicates the feedback equation:

$$F = \overline{C}E + C\overline{E}$$

Considering that the mod. 2 sum is "0" if C and E are equal and "1" if they differ, the counting sequence can be written. The jump term can be seen to be:

1 0 1 0 1

A $\overline{B}$ C $\overline{D}$ E

because if the next clock pulse enters a "1" into the first stage, the count will be:

1 1 0 1 0

The jump terms can be taken from Table II in connection with the maximum length feedback term given in Table I.

COUNT	A	B	C	D	E	
1	1	1	1	1	1	
2	0	1	1	1	1	
3	0	0	1	1	1	
4	0	0	0	1	1	
5	1	0	0	0	1	
6	1	1	0	0	0	
7	0	1	1	0	0	
8	1	0	1	1	0	
9	1	1	0	1	1	
10	1	1	1	0	1	
11	0	1	1	1	0	
12	1	0	1	1	1	
13	0	1	0	1	1	
14	1	0	1	0	1	
15	0	0	1	0	1	
17	0	0	0	1	0	
18	0	0	0	0	1	
19	1	0	0	0	0	JUMP OF 10
20	0	1	0	0	0	
21	0	0	1	0	0	
22	1	0	0	1	0	
23	0	1	0	0	1	
24	1	0	1	0	0	
25	1	1	0	1	0	
26	0	1	1	0	1	
27	0	0	1	1	0	
28	1	0	0	1	1	
29	1	1	0	0	1	
30	1	1	1	0	0	
31	1	1	1	1	0	

Figure 62. Divide-by-21 Shift-Register Generator Counter Count Sequence

Table II. Jump Terms For Non-MLS Counters

CYCLE LENGTH		A	B	C	D	E	F	(NOTE 1) J–K
	4	0	1	1				1
	5	1	0	0				1
	6	1	1	0				0
$2^n - 1$	7			MLS				
	8	0	1	1	0			0
	9	0	1	0	0			1
	10	1	1	0	0			1
	11	0	0	1	1			1
	12	1	0	0	0			1
	13	1	0	1	1			1
	14	1	1	1	0			0
$2^n - 1$	15			MLS				
	16	1	1	0	1	0		1
	17	1	0	0	0	1		0
	18	0	0	0	1	1		0
	19	0	1	1	0	1		1
	20	1	1	1	0	0		0
	21	1	0	1	0	1		1
	22	0	1	1	1	1		1
	23	1	1	0	0	1		0
	24	0	0	1	1	0		0
	25	1	0	0	1	0		1
	26	0	0	1	0	1		1
	27	1	0	1	1	0		0
	28	0	1	0	1	1		0
	29	0	1	0	1	1		
	30	1	1	1	1	0		0
$2^n - 1$	31			MLS				
	32	0	0	1	1	1	0	0
	33	1	1	0	0	1	0	0
	34	0	0	1	0	0	0	1
	35	0	1	0	1	1	1	1
	36	0	0	1	1	0	1	0
	37	1	1	1	1	0	1	0
	38	0	1	0	1	0	1	0
	39	0	1	1	1	1	1	1
	40	0	1	1	0	0	1	0
	41	1	0	1	0	0	0	1
	42	1	0	1	1	1	1	1
	43	0	0	0	1	0	0	1
	44	1	1	0	0	0	0	1
	45	1	1	0	1	0	0	1
	46	1	0	0	1	0	1	0
	47	1	0	0	1	1	1	1
	48	1	1	1	0	1	1	1
	49	1	0	0	0	1	1	1
	50	0	1	1	1	0	0	1
	51	0	0	0	1	1	0	0
	52	1	0	1	1	0	1	0
	53	0	1	0	0	0	0	1
	54	1	1	1	0	0	1	0
	55	0	0	1	0	1	0	0
	56	0	1	1	0	1	0	0
	57	0	0	0	0	1	1	1
	58	1	0	0	0	0	0	1
	59	1	1	0	1	1	0	0
	60	0	1	0	0	1	1	1
	61	1	0	1	0	1	1	1
	62	1	1	1	1	1	0	0
$2^n - 1$	63			MLS				

NOTE 1 THE TERM UNDER J–K SHOWS THE BIT TO BE ENTERED INTO THE FIRST STAGE WITH THE NEXT CLOCK PULSE.

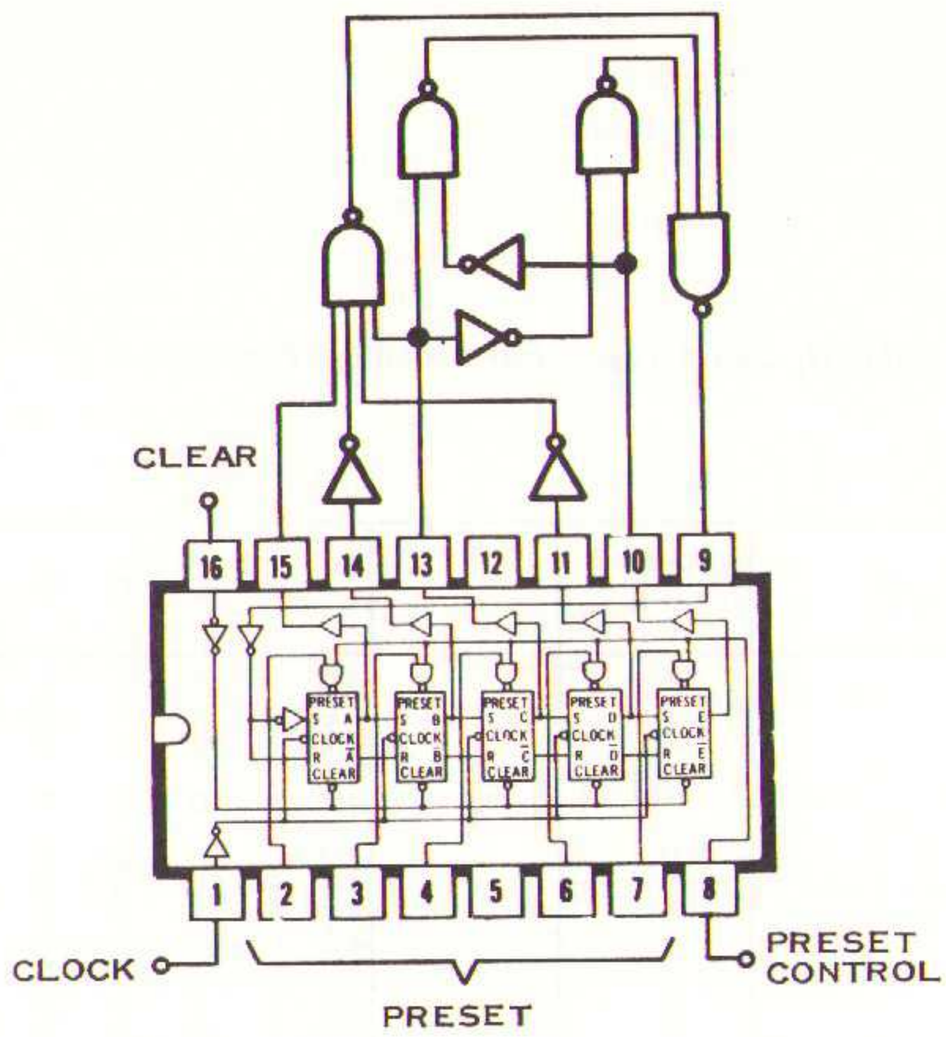


Figure 63. Divide-by-21 Shift-Register Generator Counter Using SN7496

Feedback equation for N = 21:

$$F = \underbrace{E\overline{C} + \overline{E}C}_{\text{MLS}} + \underbrace{A\ \overline{B}\ C\ \overline{D}\ E}_{\text{Jump Term}} = \underbrace{E\overline{C} + \overline{E}C + A\ \overline{B}\ C\ \overline{D}}_{\text{Simplified}}$$

See Figure 63.

Another method of finding the jump term can be described as follows:

Set the register in the all "1" state. The feedback stages are known from Table I. Considering the fact that the mod. 2 sum of ("0", "0") or ("1", "1") is "0" and the mod. 2 sum of ("0", "1") or ("1", "0") is "1", the complete cycle sequence can be written.

Assume a four bit register.

Table I indicates that feedback has to be provided from the stages C and D. The count sequence is as shown in Figure 64.

A B C D – INITIAL STATE

0 1 0 1 1 0 0 1 0 0 0 1 1 1 1 0 1 0 1 1 0 0 1 0 0 0 1 1 1 1

Figure 64. Count Sequence

Maximum length is 15 counts.

Assume a divide-by-10 counter is desired. From that follows 15-10 = 5. Five counts have to be jumped. Omit the first five bits of the initial count sequence and write this sequence below the original sequence as shown in Figure 65.

Form the mod. 2 sum of both sequences (add), enter a "zero" when the bits in both rows are equal; enter a "one" when they differ.

The jump term is that 4-bit word in the upper row for which the lower row reads 0 0 0 1. The 4-bit words of the upper and middle row differ in one bit position only.

The all zero state can be inhibited by detecting that state and presetting the counter asynchronously to the all "1" state or adding the all "0" AND term to the feedback equation:

$$F = \underbrace{E\overline{C} + \overline{E}C}_{\text{MLS Feedback}} + \underbrace{A\ \overline{B}\ C\ \overline{D}\ E}_{\text{Jump Term}} + \underbrace{\overline{A}\ \overline{B}\ \overline{C}\ \overline{D}\ \overline{E}}_{\text{Prevent all zero state}}$$

which simplifies to:

$$F = C\overline{E} + A\ \overline{B}\ C\ \overline{D} + \overline{A}\ \overline{B}\ \overline{D}\ \overline{E}$$

Implement this equation.

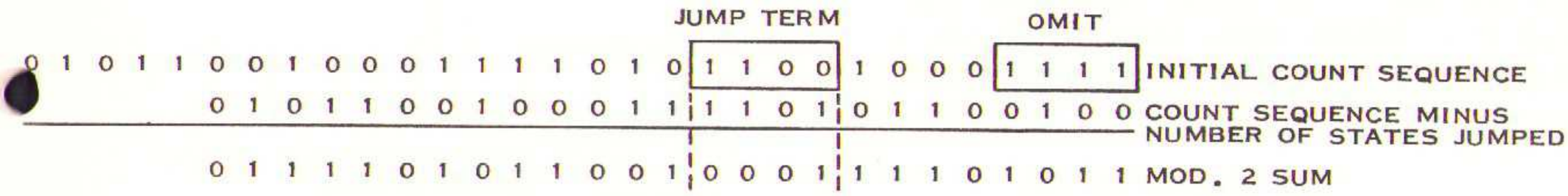


Figure 65. Jump Term

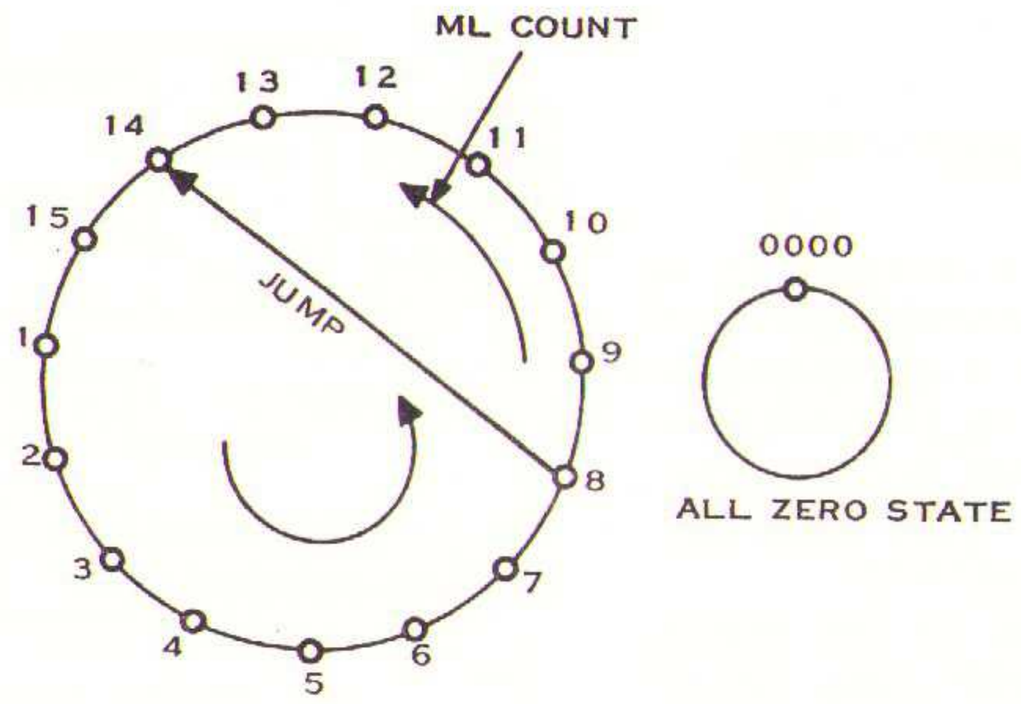


Figure 66. Divide-by-10 Cycle (All-Zero State Inhibited)

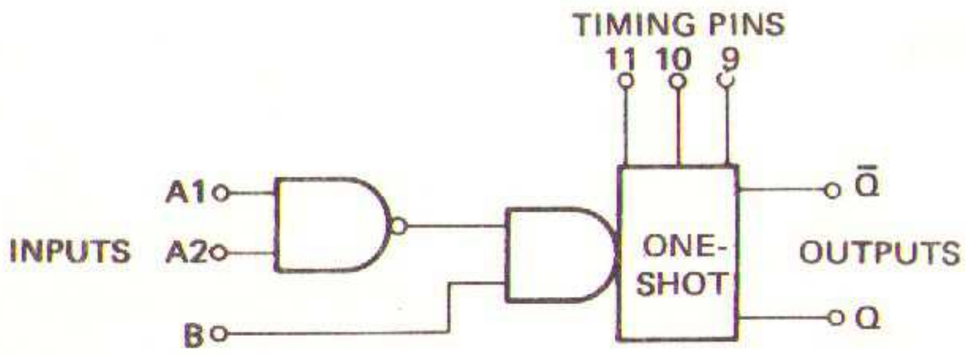
TTL ONE-SHOT: SN74121

Bob Parsons and John Slomkowski*

The SN74121 is a high-performance integrated-circuit monostable multivibrator or "one-shot" in the 54/74 TTL series. Its inputs and outputs are compatible with other integrated circuits of this series and consequently with those of several other digital IC series. This application report describes the SN74121 briefly and shows how to use it in several typical applications. Detailed specifications of the SN74121 are found in the appropriate data sheet.

SIMPLE MONOSTABLE APPLICATION

The block diagram of the monostable is given below in Figure 1. A1 and A2 are negative-edge-triggered logic inputs. B is a Schmitt input which triggers on a positive-going voltage that can be of step or ramp form.



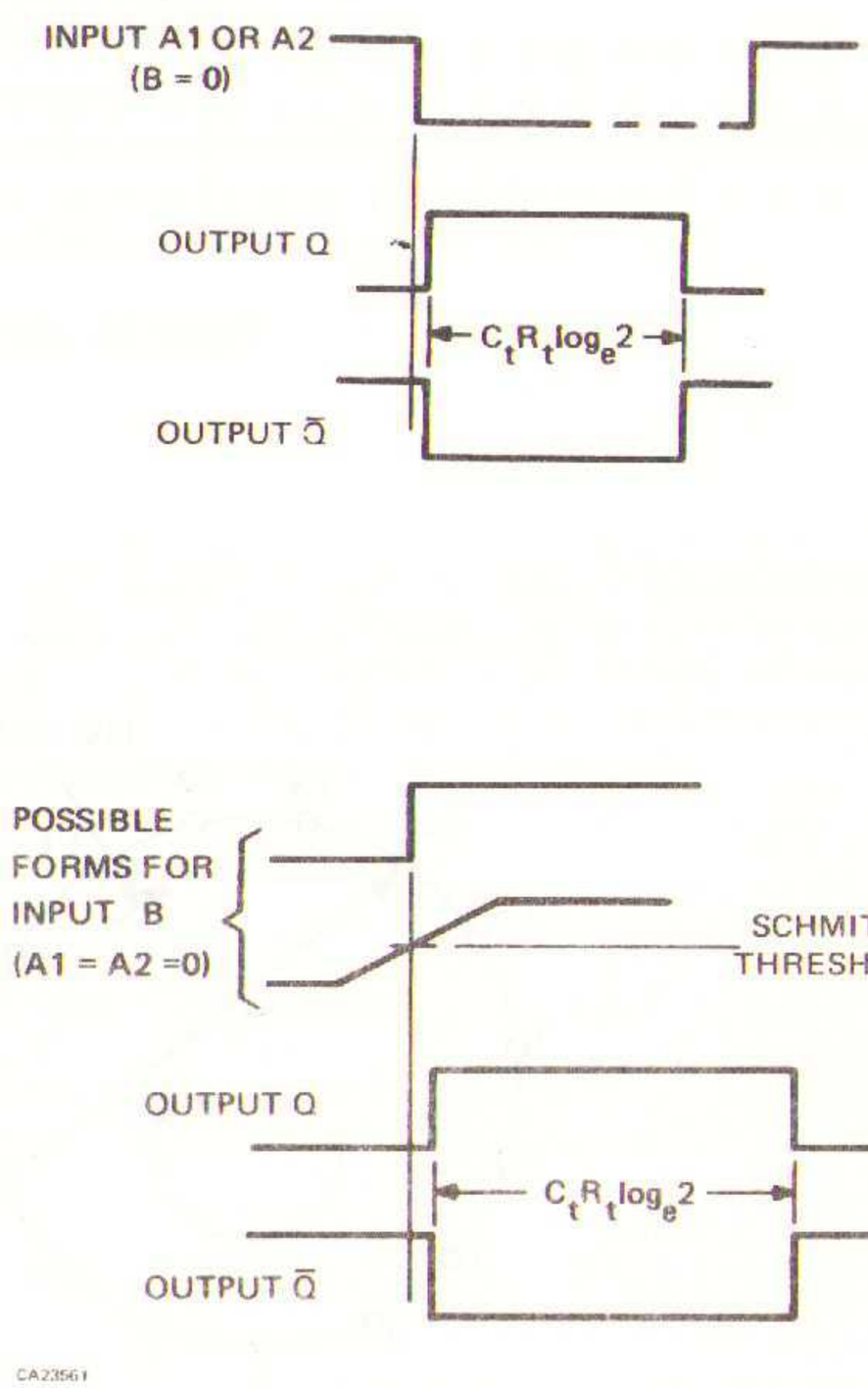
CA23560

FIGURE 1. Functional Diagram of SN74121

For use as a normal monostable, the internal timing resistor may be used. An external resistor and capacitor are used if output pulses longer than 50 ns are required. The output pulse width is given by $C_tR_t\log_e 2$. Unused inputs should be taken to a logical "1" in order to minimize stray capacitance associated with them. If input B only is used, then A1 or A2 must be taken to a logical "0".

The maximum allowable value of the external capacitor C_t is determined by capacitor leakage and the duty cycle required. In practice, leakage limits the value of capacitor C_t to approximately 1,000 μF. The maximum charging current for it is limited to approximately 65 mA for a V_{CC} of 5 V, and the typical value is 35 mA.

Waveforms which show the normal operation as a monostable are given in Figure 2. The Schmitt input trigger level is approximately equal to 1.5 V. Noise present on the edge can not turn the Schmitt off again unless it occurs in less than 30 to 50 ns and is greater than the 200-mV "backlash".



CA23561

FIGURE 2. Wave forms for SN74121 Operating Alone as a Monostable Element

*Texas Instruments Limited, Bedford England

MONOSTABLE WITH INPUT DELAY

The positive ramp-triggered Schmitt input B can be used with a capacitive-resistive network to give input delay, as shown in Figure 3. The waveforms associated with the operation of this circuit are shown in Figure 4.

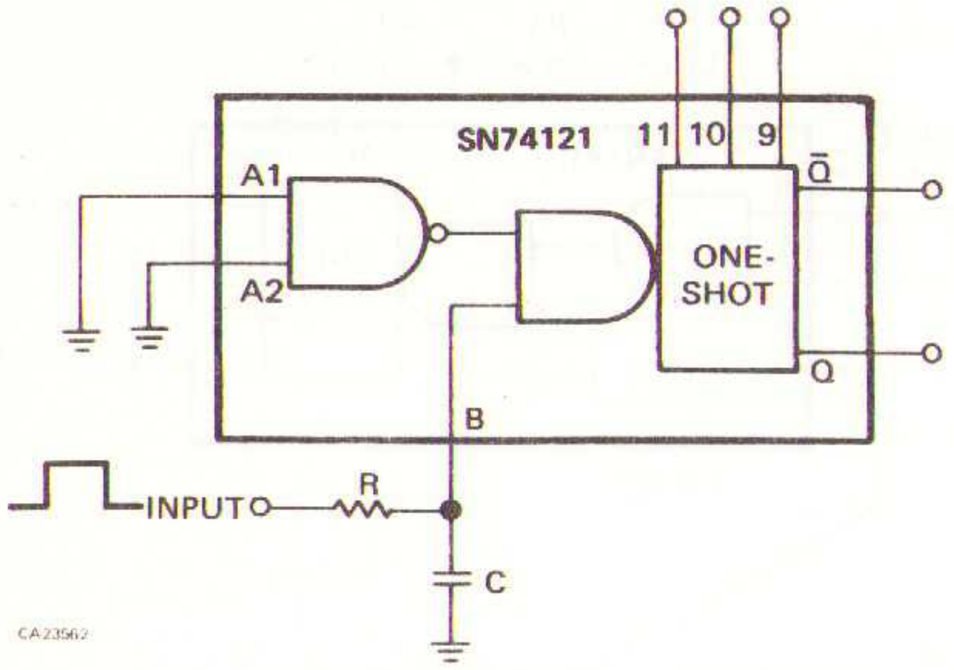


FIGURE 3. Simple Method of Delaying a Pulse at the Schmitt Input

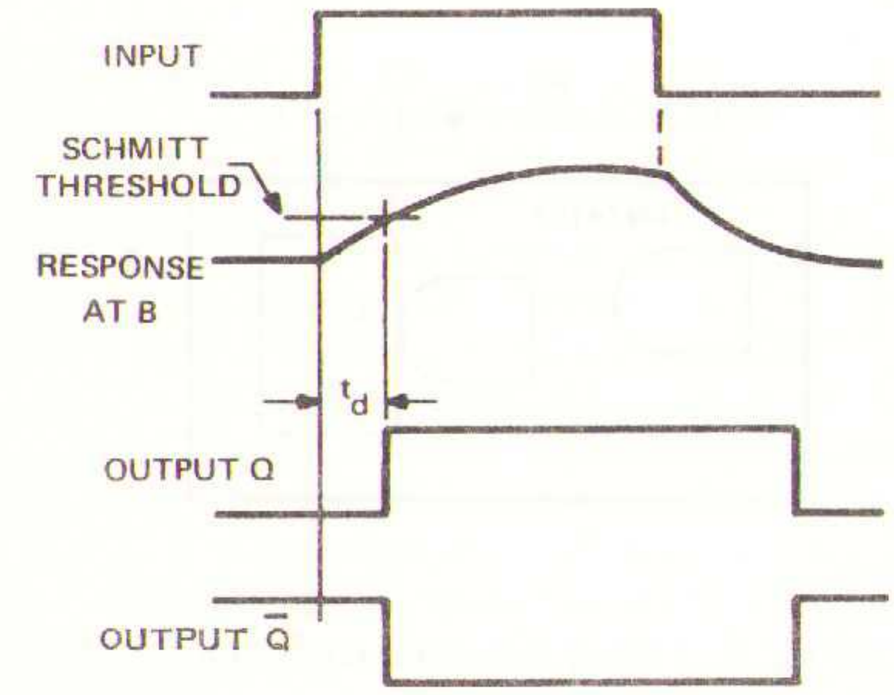
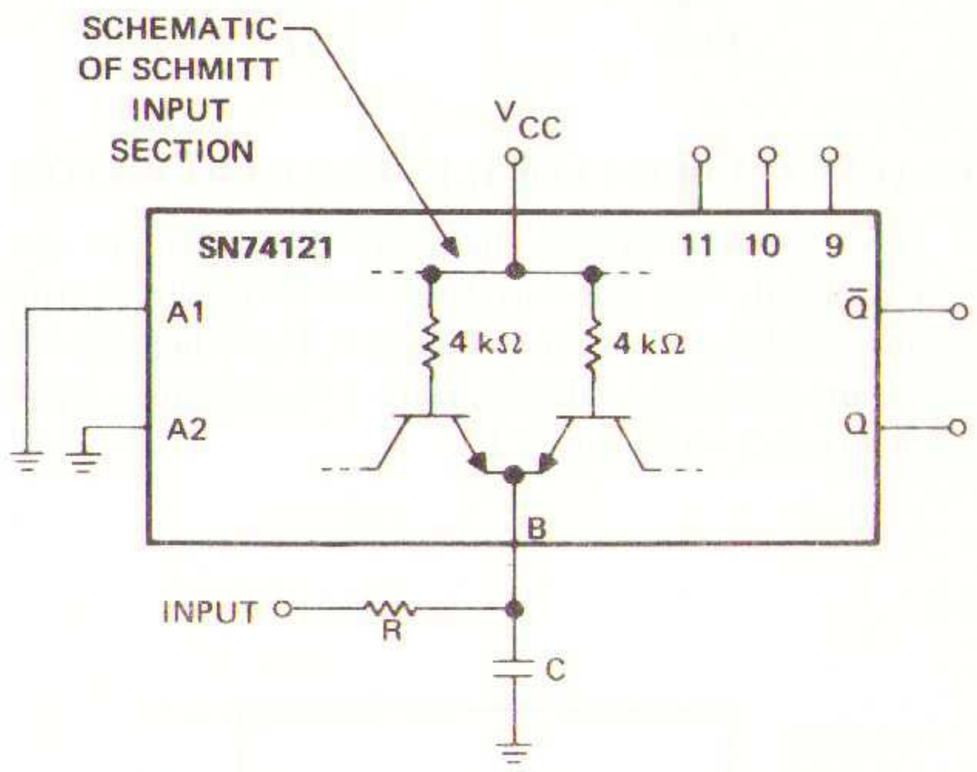


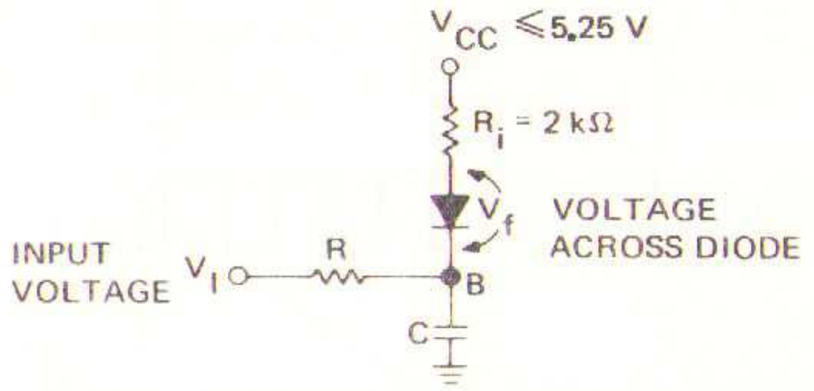
FIGURE 4. Delayed Output from Circuit in Figure 3

When the input changes from a logical "0" to a logical "1", capacitor C charges towards the logical "1" potential. After a time t_d, the voltage across capacitor C reaches the Schmitt trigger level and fires the monostable, producing an output from Q.

In order to prevent the monostable from firing when the input signal is a logical "0", R should be limited to a certain maximum value. Figure 5 shows how the maximum permissible inhibiting voltage at B (0.8 V) and the internal circuitry of the Schmitt input determine the maximum value of R. The voltage V_B at B, which is $[(V_{CC} - V_f)\,R + V_I R_i]/(R + R_i)$, must not exceed 0.8 V. Therefore the maximum permissible value of R is $(V_B - V_I)\ (R_i)/(V_{CC} - V_f - V_B) = (0.8 - 0)\ (2000)/(5.25 - 0.7 - 0.8) = 427\ \Omega$. Capacitor C has a maximum value which is determined by the duty cycle of the input waveform and the value of resistor R, as it must be discharged before the next cycle can commence.



(a) RELATION OF INTERNAL SCHMITT CIRCUITRY TO DELAYING CONNECTION



(b) SIMPLIFIED EQUIVALENT OF CIRCUIT ABOVE

CA23564

FIGURE 5. Basis for Determining Maximum Permissible Value of Delaying Resistor in Figure 3

The delay time t_d is directly proportional to the value of capacitor C. However, it is not directly proportional to the value of resistor R but a function of $(R + r)$ where r is the output impedance of the driving stage when in the logical "1" state (typically 130 Ω). There is no simple relation between resistance R and the delay time due to the Schmitt input current flowing through R. Table I shows

typical values of t_d for R = 100 Ω with various values of C. These time delays are repeatable in practice.

Table I. Measured Time Delays for Various Capacitances in Delay Circuit of Figure 3

t_d (μs)	C (nF)
1.36	10
2.50	20
4.90	40
12.46	112

STABLE GATED CLOCK PULSE GENERATOR

For some applications, the waveforms shown in Figure 6 are required. This gate waveform can be generated using two monostables as shown is Figure 7. Here there are two gate inputs available as shown, Gate 1 enabling on a logical "0" and Gate 2 on a logical "1".

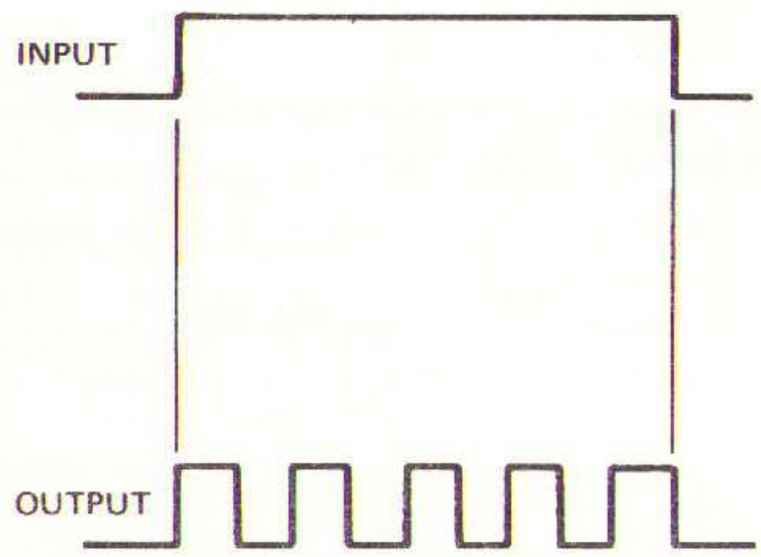


FIGURE 6. Clock Signal Generated by Circuit in Figure 7

The waveforms during the operation of this circuit are shown in Figure 8 below. The times t_1 and t_2 are determined by the time constants R1C1 and R2C2 respectively.

A DIGITAL FREQUENCY-TO-VOLTAGE CONVERTER

Pulse-counting discriminators exist that use the basic principle of a method first described by Scroggie, but discrete-component circuits require many transistors, some of which must have a very high switching speed to produce a low-distortion output. A practical method of detecting frequency modulation is possible using three integrated circuits, one of them the monostable unit. This design is a digital frequency-to-voltage converter that does not require any inductors or the normal elaborate setting-up procedure.

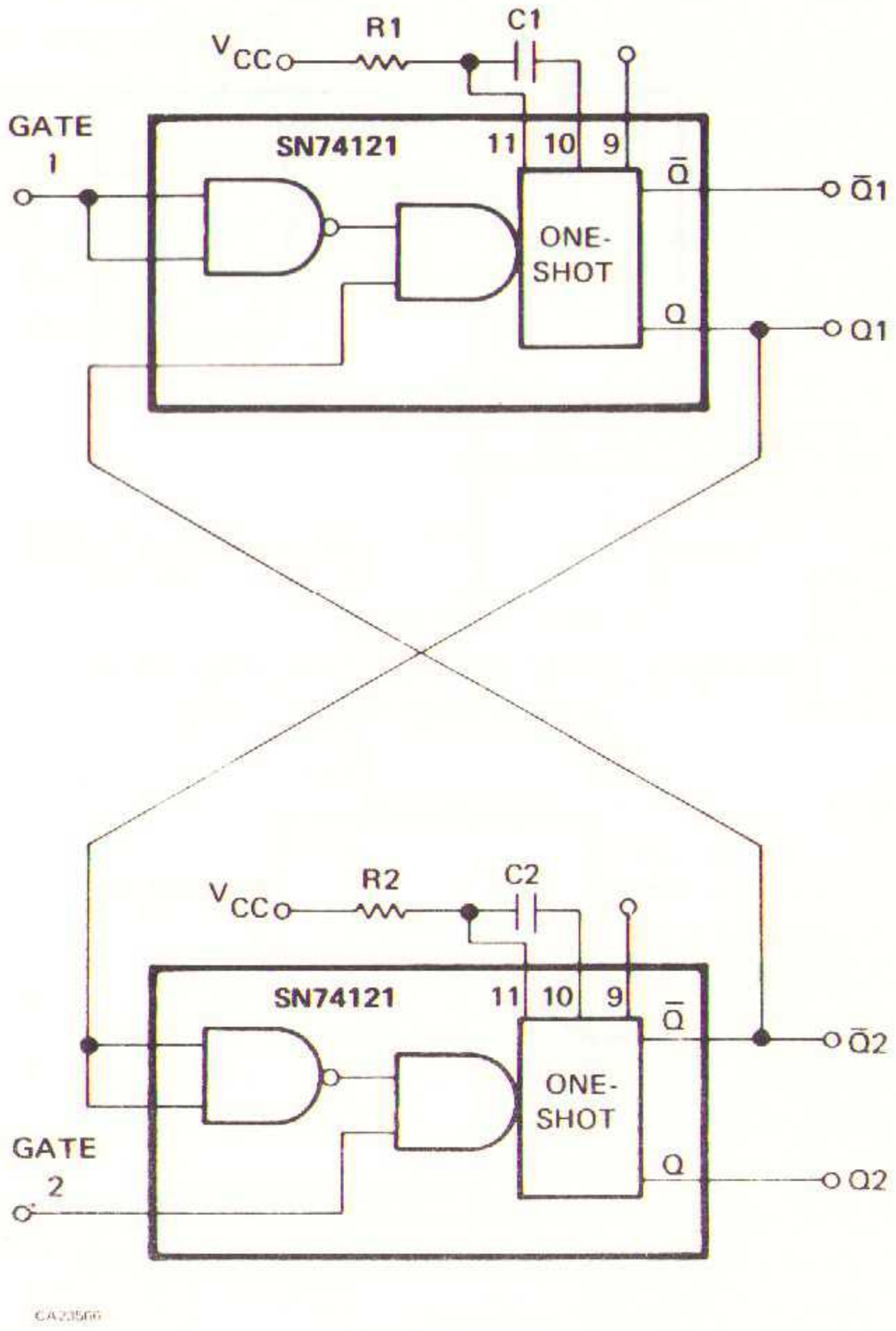


FIGURE 7. A Clock Pulse Generator Using SN74121

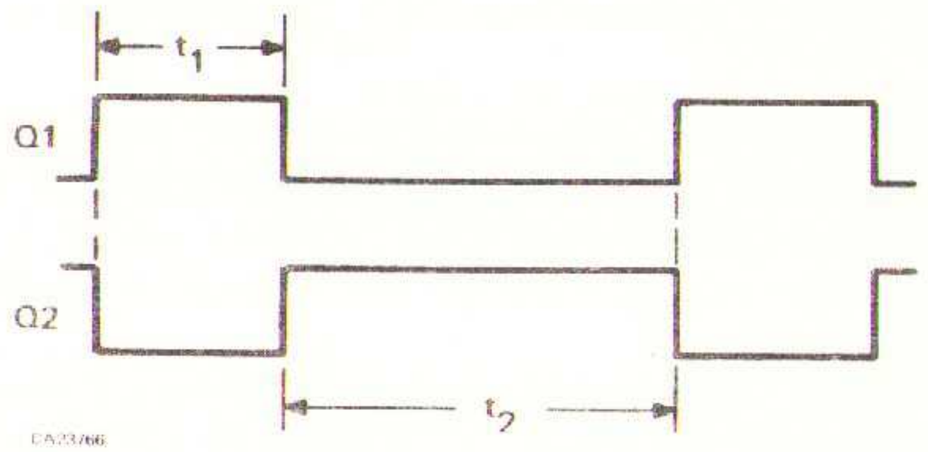


FIGURE 8. Approximate Relation of Pulses from Non-Inverting Outputs in Figure 7

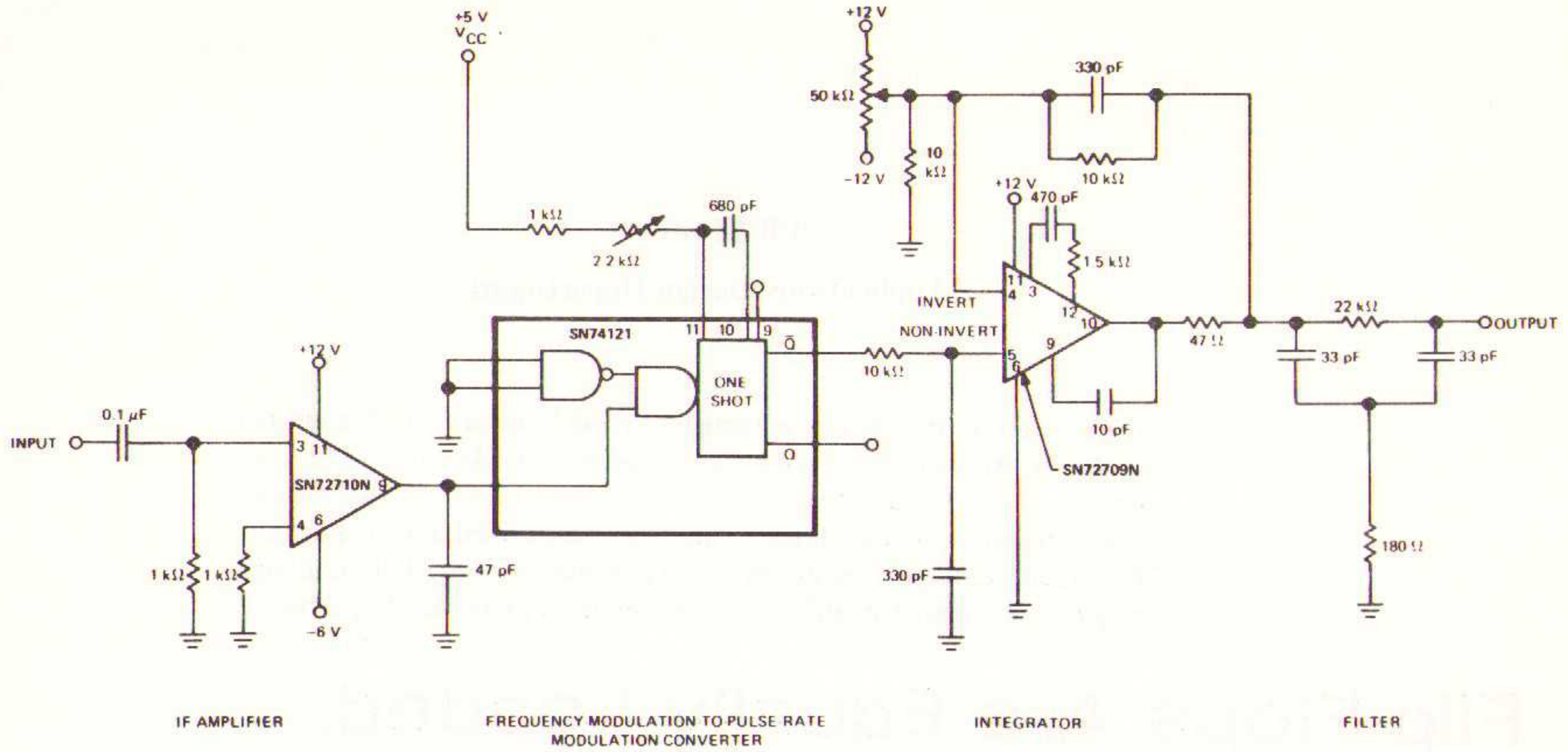


FIGURE 9. Schematic Diagram of Digital Frequency-to-Voltage Converter

The circuit diagram of the frequency-to-voltage converter is shown in Figure 9. A variable input frequency centered between 100 kHz and 600 kHz is applied to the input of the SN72710 integrated-circuit comparator. Its output, compatible with TTL, is used to trigger the SN74121 monostable circuit. Constant-width pulses are produced at a rate determined by the input frequency. Very stable pulse widths are obtained since the monostable circuit is internally compensated for temperature changes and the timing components are external to the network. The timing resistor is adjusted to give the best linearity for the input frequency range.

The constant-width pulses are then integrated by an SN72709. This high-gain amplifier has an advantage over a passive network in that the charging current in the integrating capacitor is constant, thereby producing a more linear transfer characteristic. Frequency compensation is applied at two points to stabilize the amplifier. The input direct current of the amplifier is balanced out by means of the 50-kΩ preset potentiometer. The output of the integrator is filtered through a bridged-T network to attenuate the remaining high-frequency carrier component.

The transfer characteristic for the system from 100 kHz to 600 kHz is shown in Figure 10. For a deviation of ±80 kHz relative to 200 kHz, the system has a linearity of 0.9%.

When used as an FM discriminator, the system gives an audio bandwidth (−3 dB) of 6 Hz to 33 kHz.

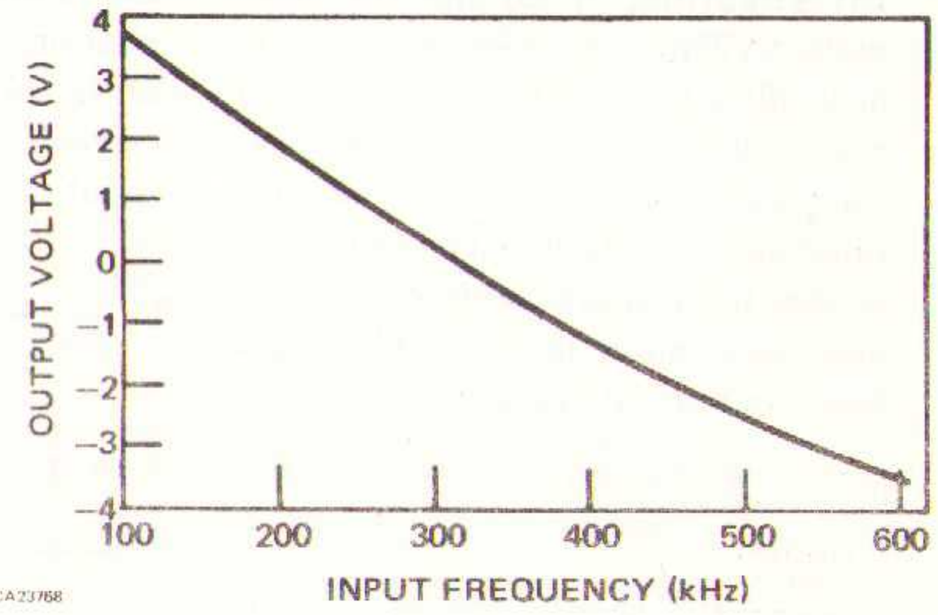


FIGURE 10. Transfer Characteristic of Converter in Figure 9.

TTL DESIGN CASES AND GUIDELINES

Bill Heniford

Applications/Design Department

The first seven items herein are articles by Bill Heniford which appeared in the "Customer Engineering Clinic" section of EDN magazine from January through April, 1969. Each article presents a 54/74 TTL "design case" consisting of a problem frequently encountered and its solution. The final item is a summary of guidelines for 54/74 TTL design prepared by several members of the Applications/Design Department.

Flip-Flops Are Equally Loaded, But One Fails Repeatedly*

Problem: Flip-flops fail repeatedly at a specific location on a printed-wiring board. Other flip-flops on the same board identically loaded never fail. All devices are operating within data sheet limits.

Investigation: Analyzing the schematic in **Fig. 1** revealed no excessive dc loading, transient loading or power dissipation. No significant reactive components were present. Clock and input signals originated on the board, so that noise spikes seemed unlikely, and none could be detected on the board in normal operation.

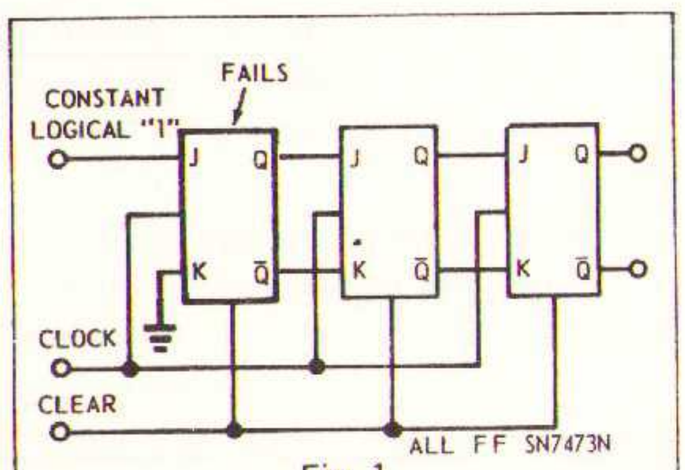


Fig. 1.

Analysis of failed devices showed evidence of excessive clock input current when a logical "1" was applied to the clock input in many cases. Nearly all failed devices showed evidence of excessive currents at the "J" input with a logical "0" or "1" applied, except for a few which appeared open.

Deduction: The "J" input seems to be the failure point, since there is some abnormal condition at this point in all failed devices. If the "J" input received a damaging power pulse, the input emitter structure at this location could short emitter-to-base, emitter-to-emitter, or a combination. In extreme cases, the bond could be damaged or the metallization vaporized.

Verification: When rechecking the schematic (**Fig. 1**), it was noted that the "J" input of the failing device is specified as a continuous logical "1". Tracing the printed board revealed that the logical "1" was implemented

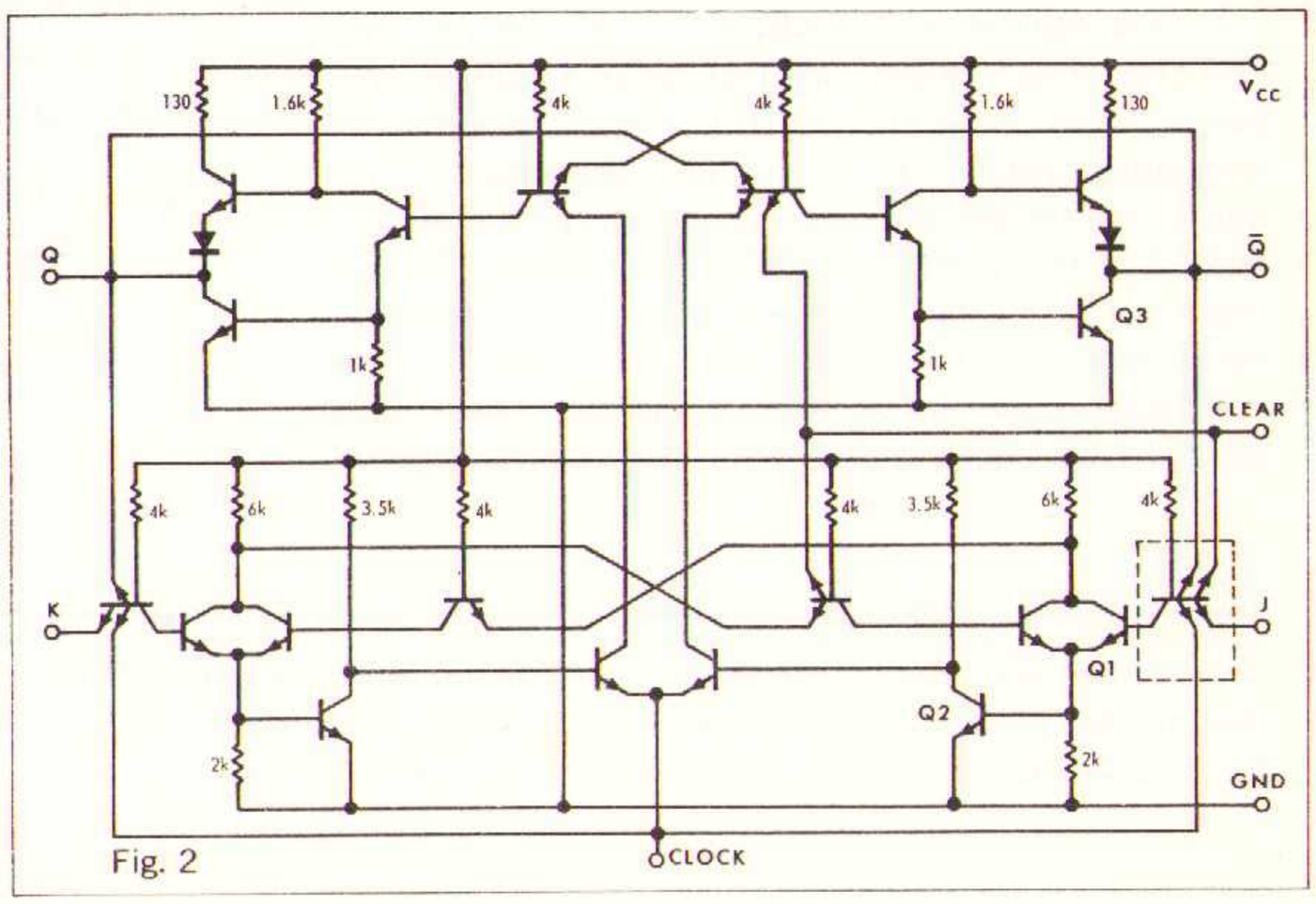


Fig. 2

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* Reprinted from the January 15 through the April 15, 1969 issues of EDN, a Cahners publication.

by tying directly to the +5V V_{cc} line, which is within the +5.5V data sheet limit for series 54/74 TTL devices. Apparently, damaging transients were coming in on the V_{cc} line, and cycling the power supply revealed an occasional turn-off transient in excess of 15V.

Analysis: The input structure of TTL integrated circuits consists almost exclusively of multiple emitters having a common base junction (**Fig. 2**). If a high positive voltage is applied to "J", this emitter may go into zener breakdown at a typical voltage of 6V. The path may be completed through path 1 to the $\bar{Q}$ output if in the "0" state, through path 2 to the clock line if the clock level is at a logical "0", or by path 3 through the clear input if the clear input is at logical "0". If none of these occurs, path 4 through the emitter-base junctions of Q1 and Q2 will be taken. In any case, the resulting equivalent circuit may be represented by **Fig. 3**. Since the highest voltage will be across the 0.64-mil² emitter junctions, a hot spot occurs, destroying the "J" junction. With the loss of the zener offsetting voltage, a sharp increase in current occurs. This in turn can damage or destroy the other junctions in the area or, in extreme cases, cause the circuit to open. **Fig. 4** describes the V-I characteristic of the series 54/74 TTL input.

Solution: The solution is to prevent excessive dissipation either by clamping the input "1" level below the specified 5.5V level or by providing current-limiting in case breakdown does occur. General rules for unused inputs, or those to which a logical "1" must be supplied are:

1. Connect to V_{cc} through a 1 kΩ current-limiting resistor. Any number of such inputs that can be grouped together conveniently may be tied to one resistor.
2. Connect to used inputs carrying the desired signal where allowable within the constraints of logic level and fan-out.
3. Connect all of the inputs of a surplus NAND gate to ground and use the resulting logical "1" output for up to 10 inputs requiring this continuous level.

Uncontrolled transients on inputs have been seen to destroy the junction in as little time as 1 μs, while the same voltage may be tolerated at the V_{cc} input for a much longer time. In one case similar to **Fig. 1**, 18V applied to V_{cc} for several seconds produced no detectable damage. However, one flip-flop where "J" and "K" were connected to V_{cc} was destroyed. □

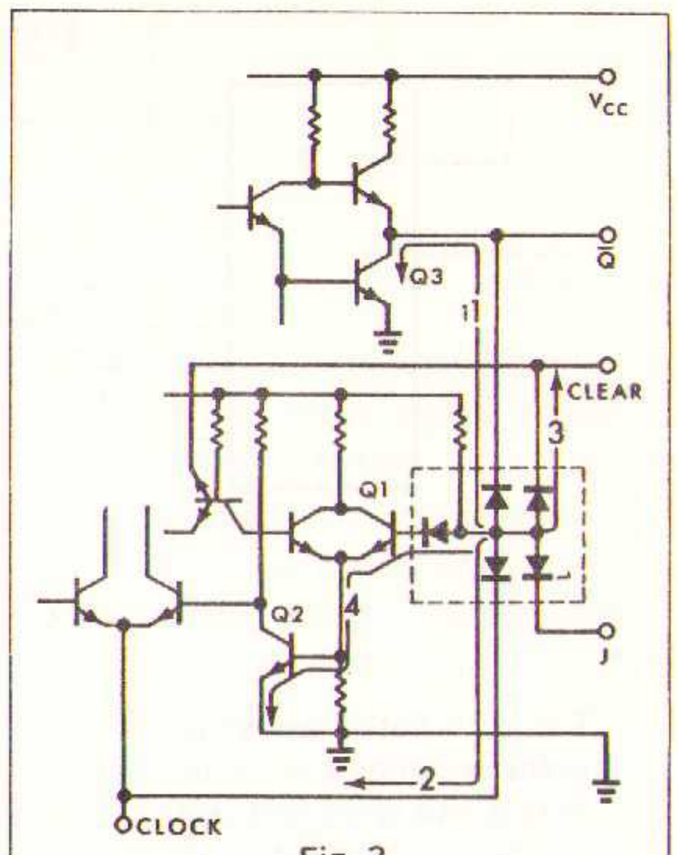


Fig. 3

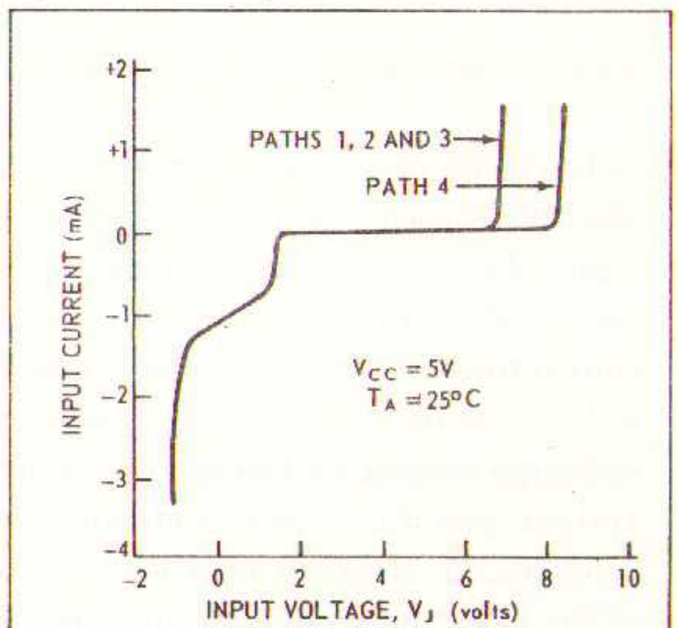


Fig. 4

One-Shot Circuits Driven from Decade Counter Give Multiple Pulses

Problem: Circuits driven by high-speed asynchronous counters produce undesired outputs (**Fig. 1**). A step is noted on the counter outputs in the "1" state and the customer assumes this to be the cause.

Investigation: The observed waveforms are normal for this device and cause no problem except for very sensitive transient-coupled circuits. Since this circuit is dc coupled with a 1.4V threshold, there must be a transient crossing the threshold that the observed waveform steps do not show.

An operational check of the circuit showed normal output triggering at the count of four (0100) with an additional output at the count of eight (1000). The output of gate 1 was observed to be approximately equal

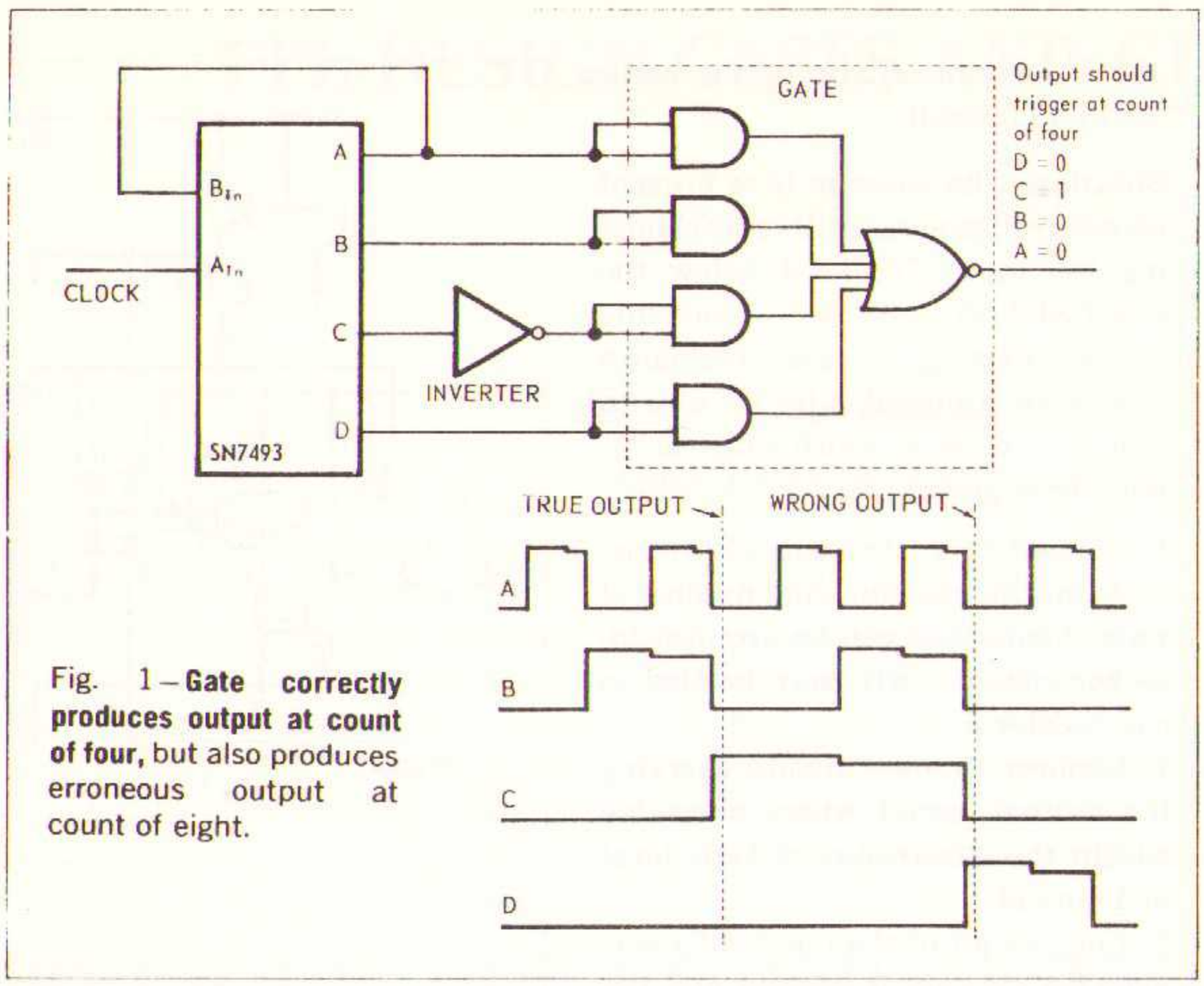


Fig. 1 – **Gate correctly produces output at count of four,** but also produces erroneous output at count of eight.

to the clock period for the normal output but was only 40 ns at the count of eight. This pulse had escaped detection in the equipment.

Deduction: Since the extraneous pulse is quite narrow, it is suspected to be generated by the timing of the system, possibly a race condition. The propagation delay from the A input to the D output can be as much as 135 ns. Since each flip-flop in the counter triggers from the preceding one, there is a possible delay of 34 ns between the fall of an output, such as B, and the response of the next stage, such as C. Thus the binary number four can recur for 34 ns. Also, the additional delay of the inverter on the C output extends the transient four persistence.

Verification: Expansion of the waveforms of **Fig. 1** at the point of transition from seven to eight **(Fig. 2)** shows that although neither seven nor eight are separated from four by less than two bit changes, there is a brief period where the count of four reappears. This coincides with the undesired output pulse.

Solution: Actually, there isn't a good solution in which gated outputs of high-speed circuits must be taken from an asynchronous counter. A synchronous circuit should be used whenever possible.

If an asychronous counter must be used, the outputs should be gated with the clock input. Since the clock falls first, it will lock out the gated output until the clock goes high again, allowing settling time for the counter. **Fig. 3** shows the revised circuit and associated waveforms at the count of eight.

It also is possible to slow the response of the gating circuit with capacitive loading at the output. Similarly, slower gating circuits such as SN15930 series DTL may be used. □

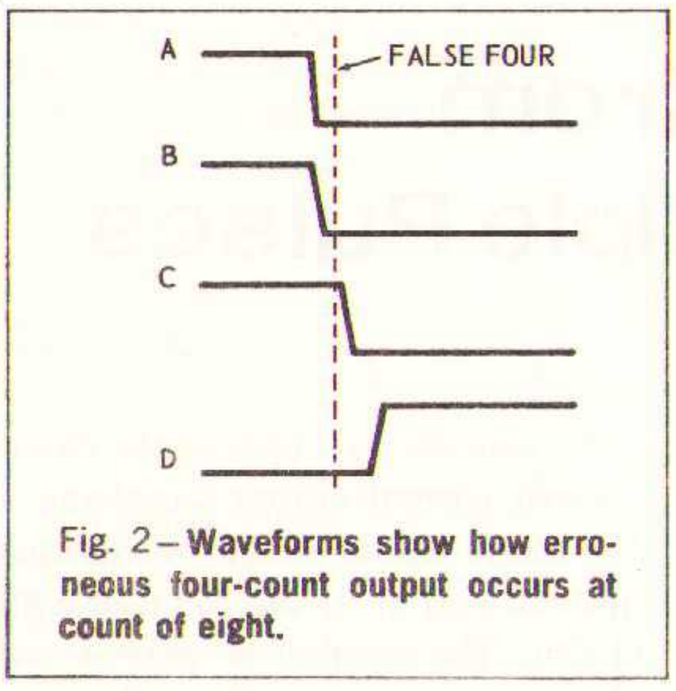


Fig. 2 – **Waveforms show how erroneous four-count output occurs at count of eight.**

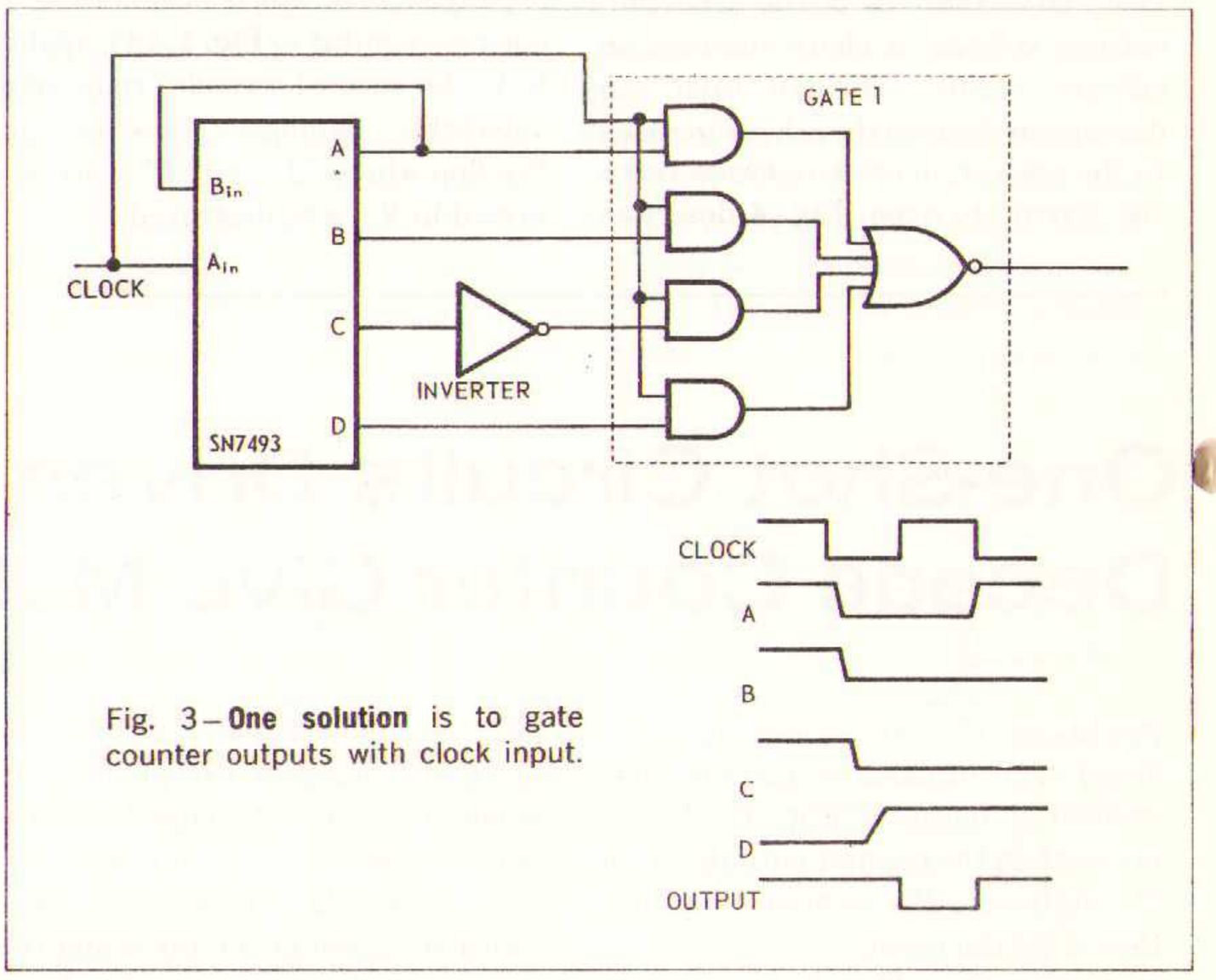


Fig. 3 – **One solution** is to gate counter outputs with clock input.

Flip-Flop Does Not Respond According to Truth Table

Problem: A TTL J-K flip-flop (SN-7473) does not respond according to the truth table. All transitions at the clock and J-K inputs are smooth and there are no detectable noise inputs. TTL gates with adequate rise and fall times drive the J, K and clock lines. Further, presets and clears are connected properly to a fixed logical 1 level.

Deduction: This flip-flop is a J-K master-slave type. It is possible that erroneous rather than desired data are being stored in the internal latch and are being transferred to the output.

Verification: The data sheet (TI Series 54, DL-S6710107) recommends that the input setup time t_{setup} be no shorter than the applied clock pulse. This recommendation appears somewhat indefinite. The true meaning of the statement is that data inputs must not change while the clock is high.

Data inputs to the circuit in question are found to be changing while the clock is high, so the circuit operates properly only part of the time.

Analysis: In the simplified logic diagram of the SN5473/7473 J-K master-slave flip-flop, two AND gates comprise the input circuit, two NOR gates make up the master latch and two NAND gates are the slave latch. Internal nodes A, B, C and D are defined to facilitate analysis of the internal sequences.

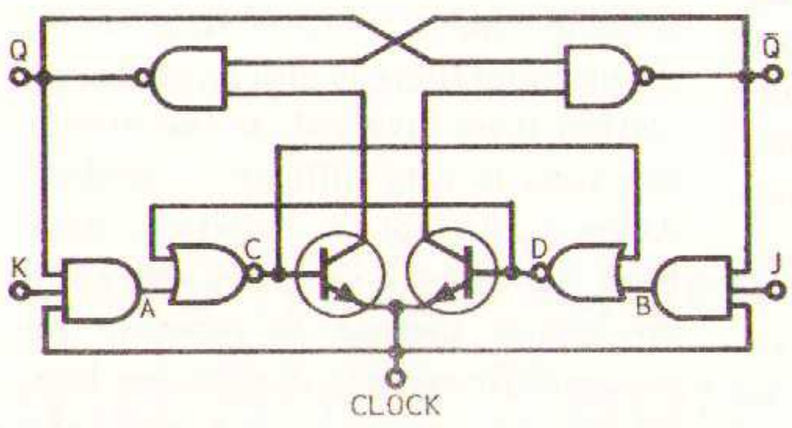
The waveforms show input changes while the clock is high at T_1, T_3 and T_5. At T_2 proper operation is obtained, but at T_4 and T_6 the response does not agree with the last data presented to the J-K inputs.

Note the master latch response (A and B) at T_1. When J goes high, C goes high and D goes low. Up to that time the master latch remained as set by the previous operations. As dictated by logical 1 levels on J and K, the output changes state. At T_3, however, K makes a forbidden transition from high to low. Looking back to the time when the clock last went high, we note that A and B responded to the J and K data, and C and D show the information to be stored. This information is not removed at T_3 as might be expected. A goes low in response to K. However, A is feeding a NOR gate input, so C is not affected because D is still high. A false output is obtained at T_4.

At T_5, another forbidden input occurs – a transient logical 1 appears on J while the clock is high. Note that C and D immediately store this information, and the return of J to zero does not destroy it. Again a false output occurs at T_6.

Solution: The pattern is clear: if a logical 1 occurs at J and/or K while the clock is high, the datum is stored regardless of later excursions of J and K, and the flip-flop will respond to the stored data. To eliminate the problem, the t_{setup} requirement may be modified in the following manner:

1. Transitions of J or K from logical 0 to 1 may occur while the clock is high, but only if 1 is the desired input.
2. Transitions of J or K to logical 0 must occur before or coincident with the clock pulse. This state must remain until clocking occurs if 0 is the desired input.

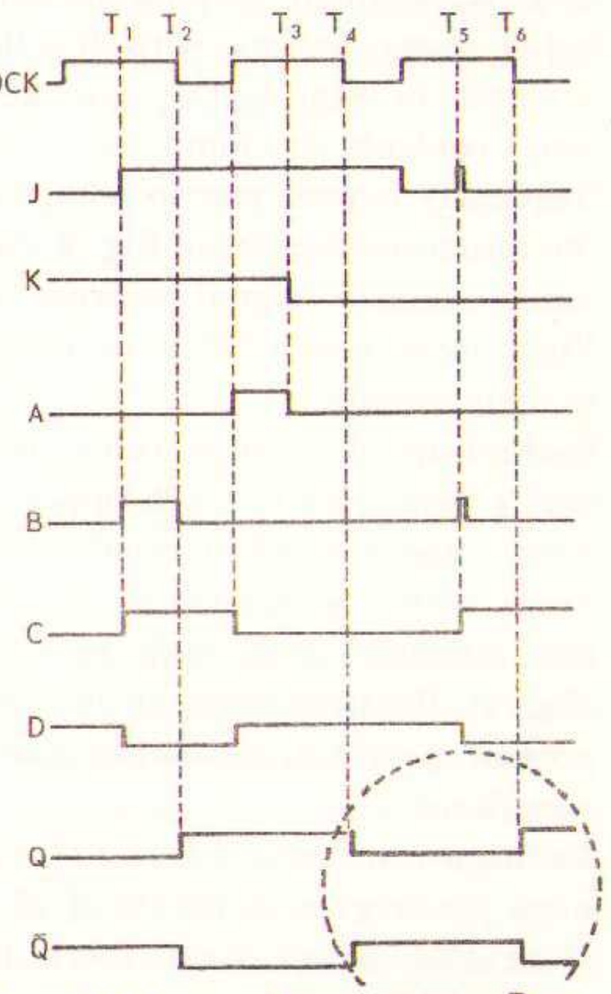


J-K TRUTH TABLE

T_n		T_{n+1}	
J	K	Q	Q̄
0	0	0	1
1	0	1	0
0	1	0	1
1	1	1	0

CIRCUIT RESPONSE

	T_n		T_{n+1}	
	J	K	Q	Q̄
T_2	1	1	1	0
T_3	1	0	0	1
T_5	0	0	1	0



J-K master-slave-type flip-flop does not respond according to truth table. Waveforms reveal source of the problem. **Dotted circles show undesired outputs.**

3. Transitions of J or K from logical 1 to 0 are permitted while the clock is high, but only if 1 is the desired input.

In the case at hand, data inputs should be modified to correct the situation if possible. Otherwise, the clock pulse width may be reduced toward the required minimum $t_{p\ (clock)}$ of 20 ns. This effectively eliminates the possibility of data change while the clock is high.

This characteristic is common to nearly all J-K master-slave flip-flops now on the market, unless a clock lockout circuit has been designed in. In a modified form, it also appears in R-S master-slave flip-flops. □

Circuits Timed from 60-Hz Line Trigger Falsely

Problem: Logic circuits that receive timing signals from a 60-Hz power source produce false outputs. Filtering the input does not improve the situation and sometimes actually makes it worse. Other circuits operating from similar sources work properly.

Investigation: Circuits driven from such sources frequently experience this problem. The problem lies in the slow rise or fall times inherent in this and many other low-frequency signals. A common method of interfacing these sources with flip-flops is shown in **Fig. 1**. The gate sometimes controls the input signals but frequently is used just to "shape up" the incoming waveform. **Fig. 2** shows some common signal sources and **Fig. 3** shows how a TTL gate responds to their signals.

Deduction: It must be remembered that a logic gate is a *saturating amplifier*, and a band of input voltage exists within which the device operates linearly with high gain (see **Fig. 4**). Because feedback is always present, potential instability must be considered.

Verification: Series 54/74 TTL gates have power gain in excess of 25 dB. With this power gain there is a bandwidth given by:

$$BW = \frac{0.35}{t_r} = \frac{0.35}{5\times10^{-9}} = 70\ \text{MHz}$$

where t_r is a typical acceptable rise time for output voltage. At such bandwidths, the stray reactances of a circuit become important. **Fig. 5** shows examples of these reactances and reveals possible feedback paths. With slow rise or fall times at the input, the logic gate may become an oscillator in the threshold region, as evidenced by **Fig. 3**.

Analysis and Cure: Theoretically, if the input signal holds the device in the linear region for a period equal to or greater than $t_{pd0} + t_{pd1}$ (characteristic gate propagation delays), oscillation could occur. There are many possible combinations of stray interactions, and there is also an oscillator startup time involved, so the unsafe rise time is very difficult to predict. Attempts to obtain empirical data have shown such variation that they are almost useless. In general, the maximum rise time depends on how "clean" the layout and decoupling are and the output impedance of the signal source. If the rise or fall time is greater than 1 μs for series 54/74, trouble should be expected.

The best solution to the slow-rise-time problem is the introduction of hysteresis with one of the circuits of **Fig. 6**. The Schmitt trigger's positive feedback introduces a "snap-action" that eliminates oscillation. **Fig. 6a** can be used with source impedances

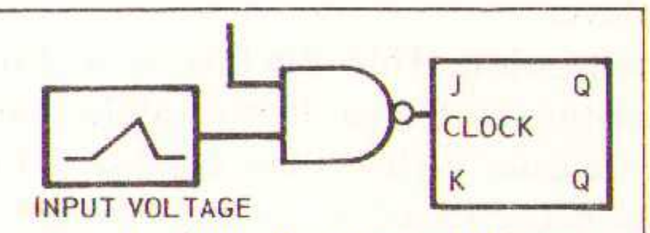


Fig. 1—**Typical method** of driving logic from slow-rise-time sources.

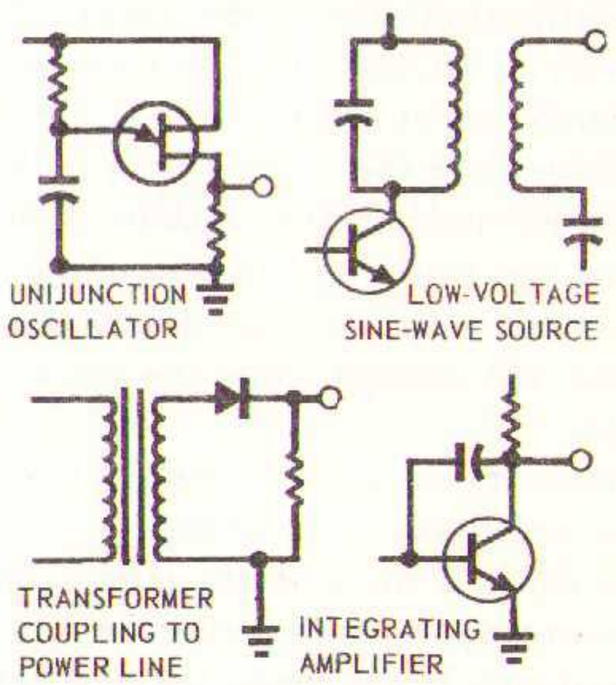


Fig. 2—
Some sources of slow-rise signals.

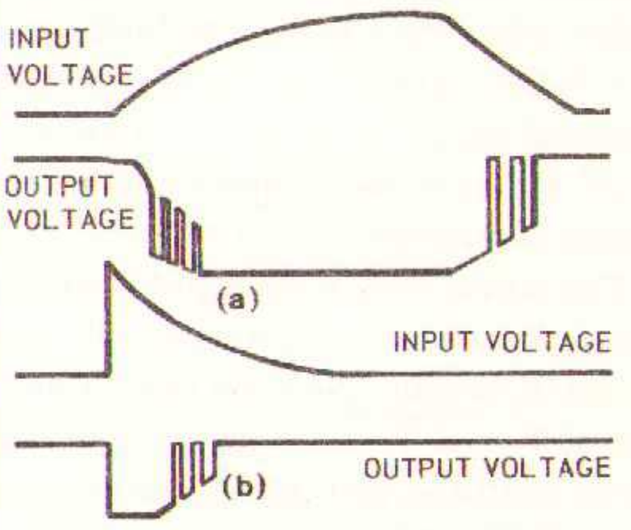


Fig. 3—**Reaction of logic gate** to **(a)** integrating amplifier drive and **(b)** UJT oscillator drive.

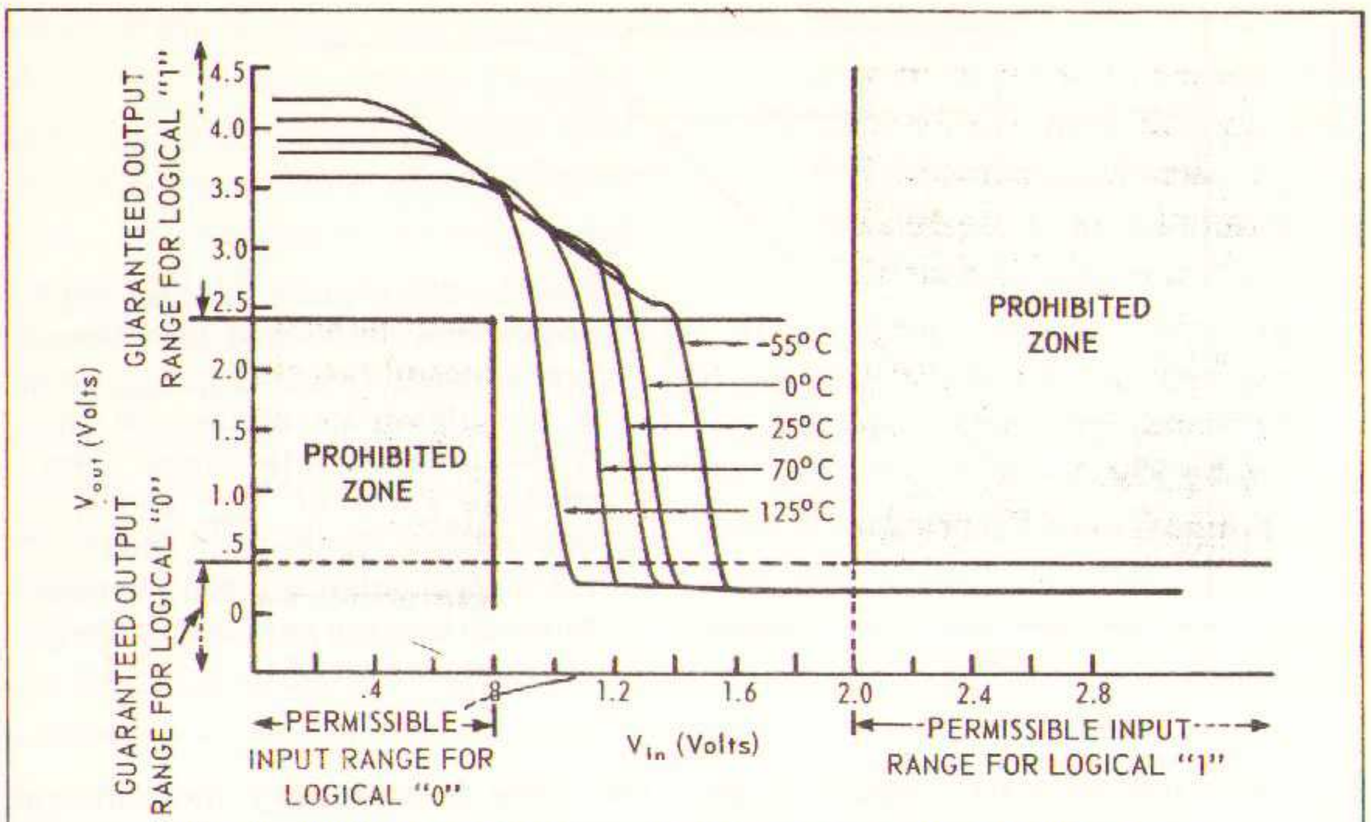


Fig. 4 – **Typical transfer characteristics** for SN5400/SN7400 gates. V_{CC} = 5.0V, fan-out = 10.

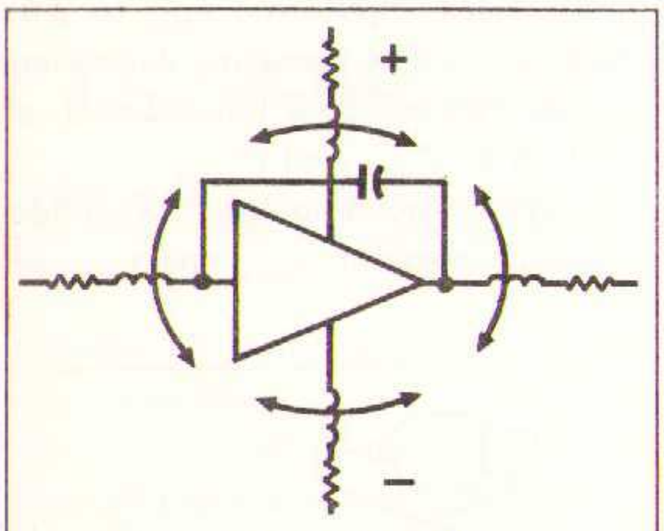


Fig. 5 – **Gate "amplifier"** showing some feedback paths.

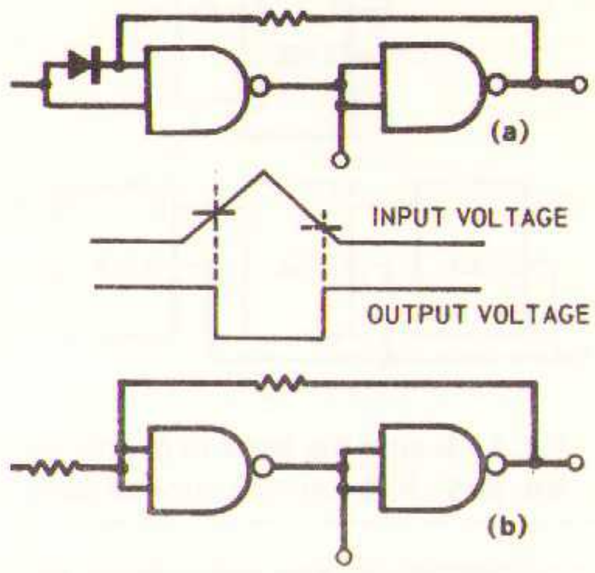


Fig. 6 – **Two TTL Schmitt trigger circuits.**

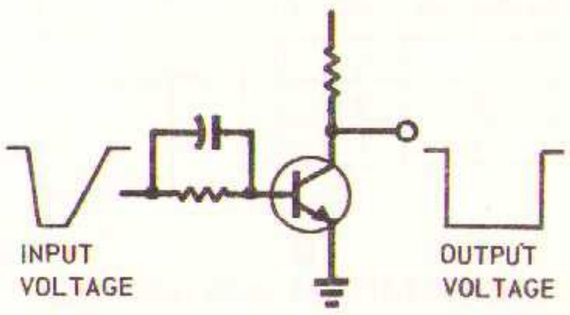


Fig. 7 – **Transistor pulse shaper.**

less than 250Ω; **Fig. 6b** is for higher impedances only. The series input resistor usually is not necessary. Inverted or noninverted outputs may be taken from either circuit.

It is also possible to shape the signal with a low-gain amplifier (**Fig. 7**) because such an amplifier is less likely to oscillate.

Oddly enough, if 54/74 TTL flip-flops are driven directly from slow-rise-time sources, no problem arises. The 54/74 TTL flip-flops, other than the SN5470/7470, are insensitive to rise time, and their latching action prevents any oscillation. ▭

D-Type Flip-Flops Mistrigger In Counters and Shift Registers

Problem: D-type flip-flops are used as binary counters in one application and as shift registers in another (**Fig. 1**). Although the clock pulse is clean and noise-free, the counter circuits often fail to trigger and the shift register sometimes fails to shift. At other times, multiple shifts occur. In both cases, unijunction oscillators supply the clock signals.

Deduction: The SN5474/7474 is a dual D-type rising-edge-triggered flip-flop. (See **Fig. 2** for truth table and block diagram.) Its operation is basically that of a latch: the data input at D is stored, then read out at Q when a clock pulse arrives. Data are both entered and transferred during the rise of the clock pulse.

Although the data sheet places no restriction on clock rise time, it does indicate setup and hold times necessary for proper operation *if* the clock pulse has a rise time of 15 ns. These parameters are defined as follows:

t_{setup}: period by which input data must precede the rise of the clock above 1.5V. No more than 20 ns is required when the clock pulse has a 15-ns rise time.

t_{hold}: period during which input data must be held following the rise of the clock above 1.5V. No more than

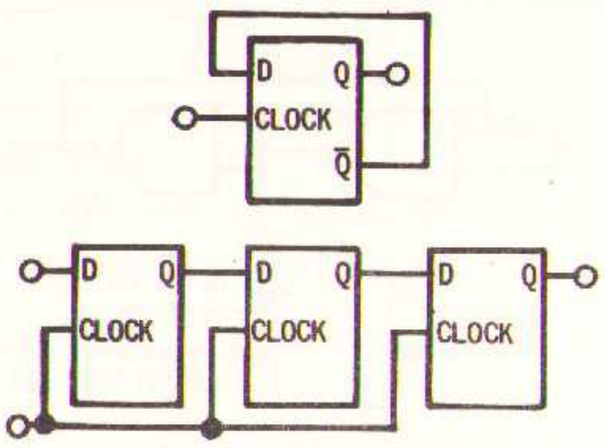


Fig. 1—D-type flip-flops in divide-by-two and shift-register applications.

BEFORE CLOCK RISE	AFTER CLOCK RISE	
D	Q	$\overline{Q}$
0	0	1
1	1	0

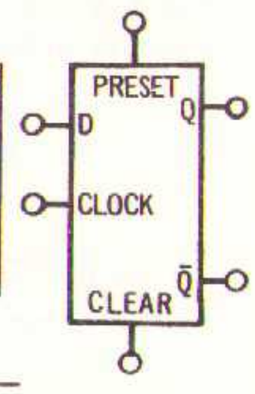


Fig. 2—
SN5474/7474 truth table and symbol

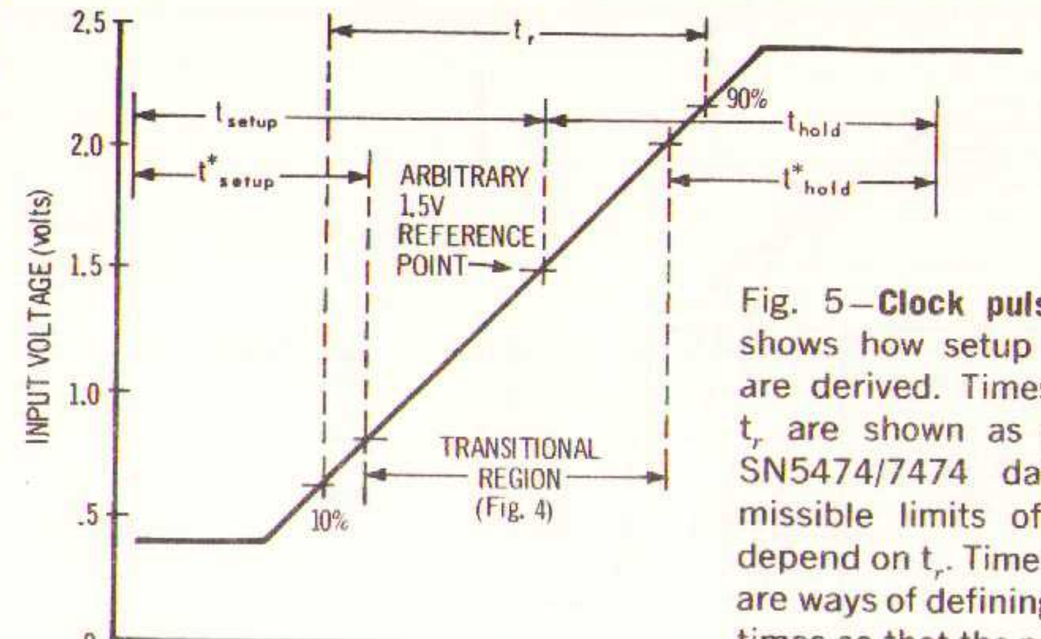


Fig. 5—**Clock pulse leading edge** shows how setup and hold times are derived. Times t_{setup}, t_{hold} and t_r are shown as defined on the SN5474/7474 data sheet. Permissible limits of t_{setup} and t_{hold} depend on t_r. Times t^*_{setup} and t^*_{hold} are ways of defining setup and hold times so that the permissible limits are independent of t_r.

5 ns are required when the clock pulse has a 15-ns rise time.

Setup and hold times inherent in the Fig. 1 applications meet data-sheet requirements—but the clock is much too slow. Herein lies the problem.

Analysis and Cure: The flip-flop is made of three interconnected latches (**Fig. 3**) that, in turn, consist of cross-coupled TTL gates. Typical gate response to an input is given in **Fig. 4.** There is an area lying between inputs of 0.8 and 2.0V known as the transitional or undefined region. Within this band, the gate is in a linear mode of operation as it changes logic states. It is also within the 1.2V input band that the flip-flop becomes active and transfers information.

The linear region of a single gate is much narrower than 1.2V, as can be seen in **Fig. 4**, and the actual transfer of data occurs at an input of approximately 1.4V at 25°C. However, this voltage depends on temperature, load and manufacturing variables, so the complete 0.8 to 2.0V input range must be considered as the transitional region in which the flip-flop transfers data.

Hold time now can be analyzed more completely; it is the time required for the two clocked gates 2 and 3 (**Fig. 3**) to rise out of the transitional zone before new data arrive. If this hold time is not observed, new data will be accepted and the circuits in **Fig. 1** will false-trigger.

Consider the clock waveforms around which t_{setup} and t_{hold} are defined. The clock rise is reproduced in **Fig. 5** with some additional points marked for clarification. With a 10- to 90-percent rise time of 15 ns, a rate of rise $\Delta V/\Delta T$ is defined:

$$\frac{\Delta V}{\Delta T} = \frac{2.16\text{V} - 0.64\text{V}}{15\text{ ns}} = 95\text{ mV/ns}$$

Assuming a linear rise, the time required to rise from the arbitrary 1.5V reference point to above the transitional region at 2.0V is:

$$T = \frac{2.0\text{V} - 1.5\text{V}}{95\text{ mV/ns}} = 5.26\text{ ns}$$

Consequently, a hold time of 5 ns is specified—but only for the defined rise time. If the rise time is extended, then t_{hold} must be increased so that the arrival of new data occurs after the clock pulse reaches 2.0V. Similar stipulation must be made for t_{setup}, but this is not the important parameter here. In summary, more instructive definitions of t_{setup} and t_{hold} would result if t_{setup} were referenced to 0.80V clock input and t_{hold} to 2.0V clock input. The resulting definitions are shown in **Fig. 5** labeled with an asterisk as t^*_{hold} and t^*_{setup}.

In applications such as the divider and shift register, t_{hold} and t_{setup} are

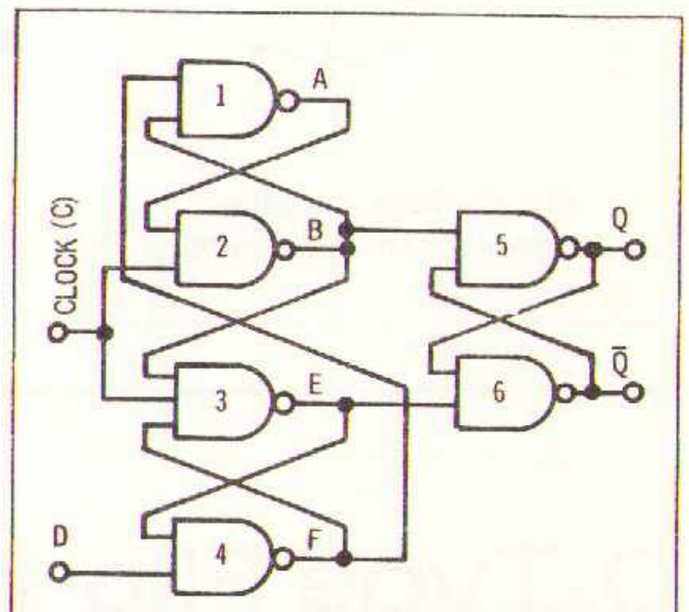


Fig. 3—**Simplified logic diagram** of SN5474/7474 flip-flop.

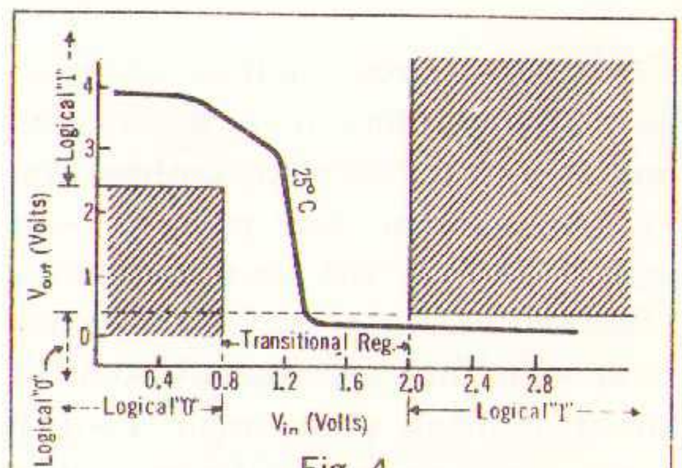


Fig. 4—
Typical TTL 54/74 gate response.

governed by the inherent propagation delays of the devices, and very little can be done to control them. Based on the minimum propagation delay, hold time and setup time from the data sheet, a maximum recommended rise time of 25 ns has been derived. Although the device is insensitive to rise time when the D input is fixed, failure to observe the 25-ns minimum produces the reactions illustrated in **Fig. 6**. The D input was fixed for the first two clock pulses and connected to $\overline{Q}$ where the waveforms are broken (See Fig. 1 divide-by-two application.) A Schmitt trigger circuit (see EDN, preceding article) is suggested to sharpen the clock signals.

A better solution is to replace the D flip-flops with J-K or R-S master-slave flip-flops. These devices have characteristics that make them ideal for counters and registers.

If it is not possible to replace the D flip-flops, a possible fix is to bypass the D input to ground with a 1000-pF capacitor. This effectively delays the arrival of the data and allows operation with a clock rise time up to approximately 500 ns. This should be considered only an emergency fix because it introduces a noisy transient current and reduces speed. □

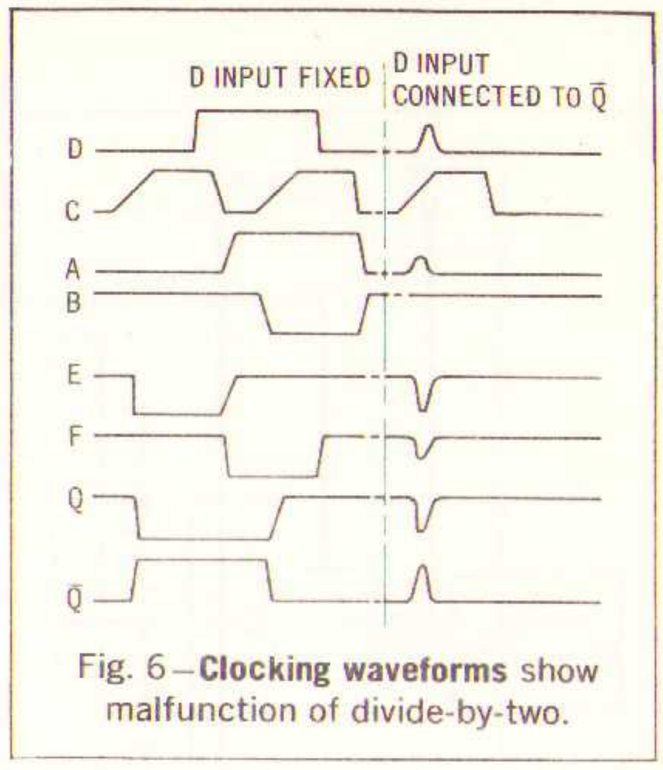


Fig. 6—**Clocking waveforms** show malfunction of divide-by-two.

TTL AND-OR-INVERT Gates Show Excessive Rise Times

Problem: AND-OR-INVERT gates with expanding inputs connected show propagation delay times far in excess of the maximum specified on the data sheet.

Investigation: With expanders connected to the expander inputs, these devices do indeed exhibit longer propagation delay. Examination of the waveform reveals that storage time (t_s) has not changed but rise time (t_r) has increased. Since propagation delay time (t_{pd1}) is a summation of storage and rise time, t_{pd1} has increased.

Verification: The data sheet specifies t_{pd1} max at 29 ns for expandable AOI gates. It also states that a total of four expander gates (SN5460) may be connected to the expander inputs. However, a necessity to hold within a t_{pd1} of 29 ns is interdictory to the use of expander gates.

The circuit used to measure t_{pd} on any standard gate is shown in **Fig. 1**. There is no indication of expander connections. Furthermore, **Fig. 2** is the setup for measuring expander propagation delay times (SN5460). Here t_{pd0} and t_{pd1} are measured in conjunction with and include the propagation delay of an SN5450 or SN5453. Although the circuit con-

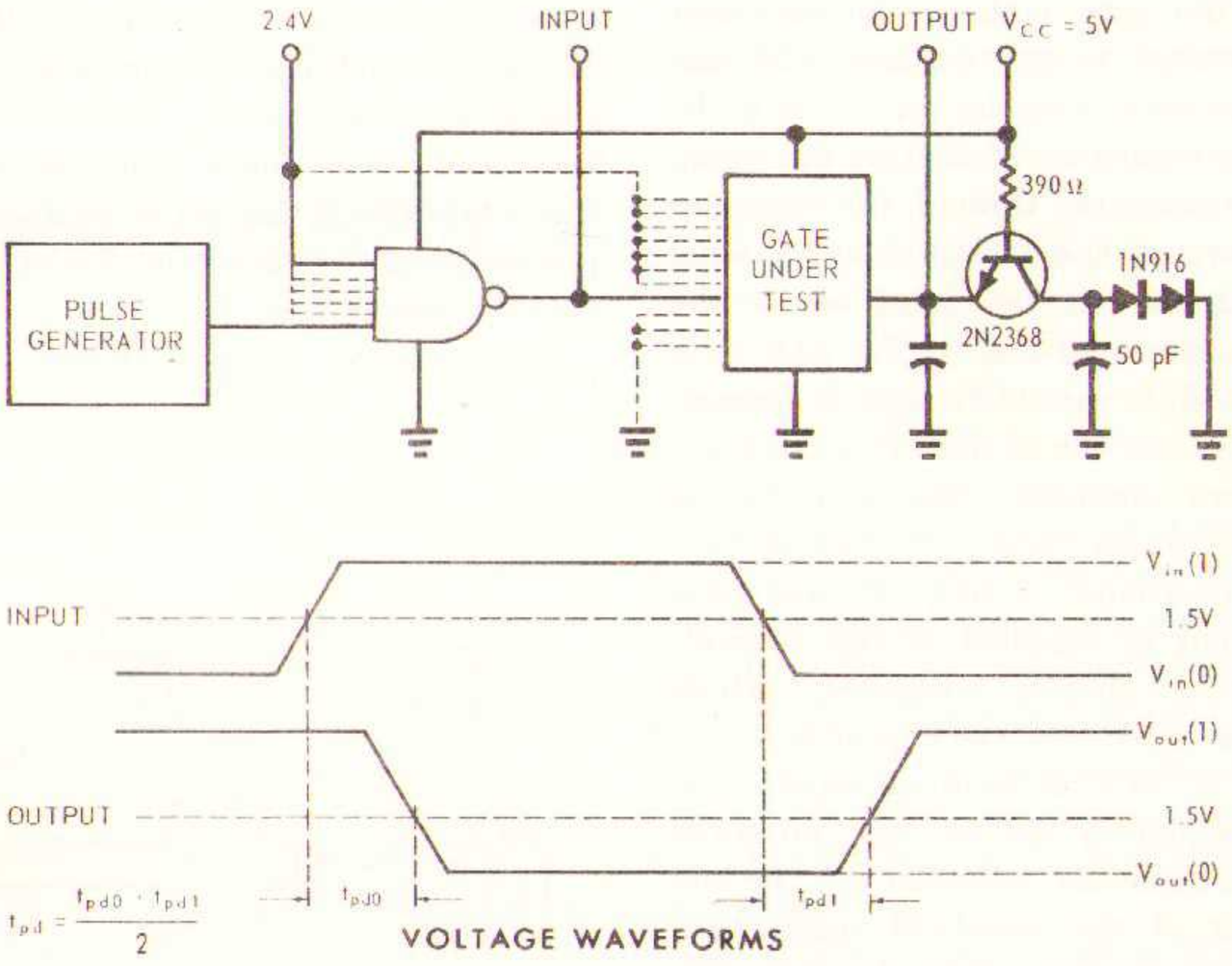


Fig. 1—**Test circuit** for measuring gate propagation delay time.

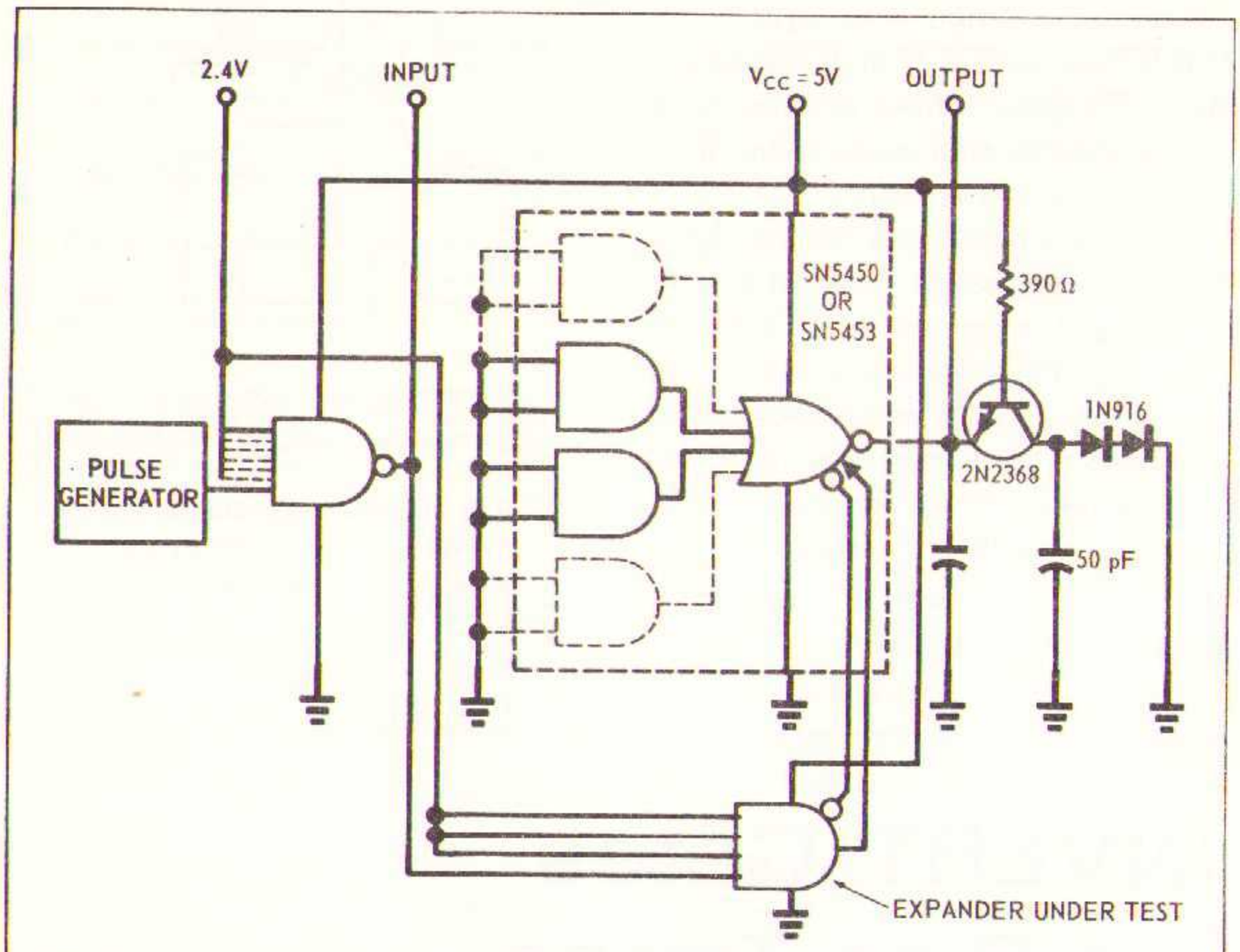


Fig. 2—**Test circuit** for measuring expander propagation delay time.

figuration is the same through the expander inputs or through the AOI gate inputs, the total propagation delay maximums are 5 ns higher than for the gate without the expander connected. In fact, the total AOI gate delay with expander connected is the same regardless of whether the signal is propagating through the expander or through the AOI gate's own inputs.

Analysis: At the point where the expander connects to the AOI gate (**Fig. 3**) a wired-OR logic is formed. When any one of the wired-OR transistors conducts, the collector is pulled down, causing the output pull-up transistor to turn off, and base current is supplied to the current-sinking output transistor, which turns on, forcing the output to a logical "0". If this condition exists, and subsequently all of the wired-OR transistors are switched off, the collector of the wired-OR transistors, which was clamped to a level consisting of the V_{BE} of the output device plus its own $V_{CE\ SAT}$, will begin to rise toward V_{CC}. The output emitter follower then will pull the output up to a logical "1".

Before this point can rise, any capacitance located there must be charged through the 1.6k resistor. Obviously, when an expander with its junction and package capacitance plus stray capacitance is connected, the rate of rise at this point is slowed. The rate of rise at the output is almost precisely equal to the rate of rise at the expander $\bar{X}$ node.

Since the data sheet indicates an increased propagation delay (t_{pd1} or t_{pd0}) of 5 ns with one expander, it is reasonable to expect at least 5 ns for each expander connected. For example, with the full complement of four expanders, an increase of 20 ns must be expected. The new $t_{pd1\ max}$ then would be 49 instead of 29 ns. Also, remember that production tests are made under conditions of minimized stray capacitance. Tests under system conditions indicate that 10 ns/expander is more realistic.

Since the increase is a voltage rate of change across a capacitance, a non-rigorous theoretical ns/pF rate can be obtained. Current through the 1.6k resistor is:

$$I = C\frac{\Delta V}{\Delta T} = \frac{V_{cc} - V_c}{R}$$

$$\frac{\Delta V}{\Delta T} = \left(\frac{V_{cc} - V_c}{R}\right)\left(\frac{1}{C}\right)$$

When the output is 0.40V

$$\frac{\Delta V}{\Delta T} = \left(\frac{5.0 - (0.40 + 0.72 + 0.73)}{1.6\text{k}}\right)\left(\frac{1}{C}\right)$$

$$= \left(\frac{3.15}{1.6\text{k}}\right)\left(\frac{1}{C \times 10^{-12}}\right) = 1.9\ \text{ns/pF}$$

When the output is 2.0V:

$$\frac{\Delta V}{\Delta T} = \frac{5.0 - (2.0 + 0.72 + 0.73)}{1.6\text{k}}\left(\frac{1}{C}\right)$$

$$= \left(\frac{1.65}{1.6}\right)\left(\frac{1}{C \times 10^{-12}}\right)$$

$$= 1.03\ \text{ns/pF}$$

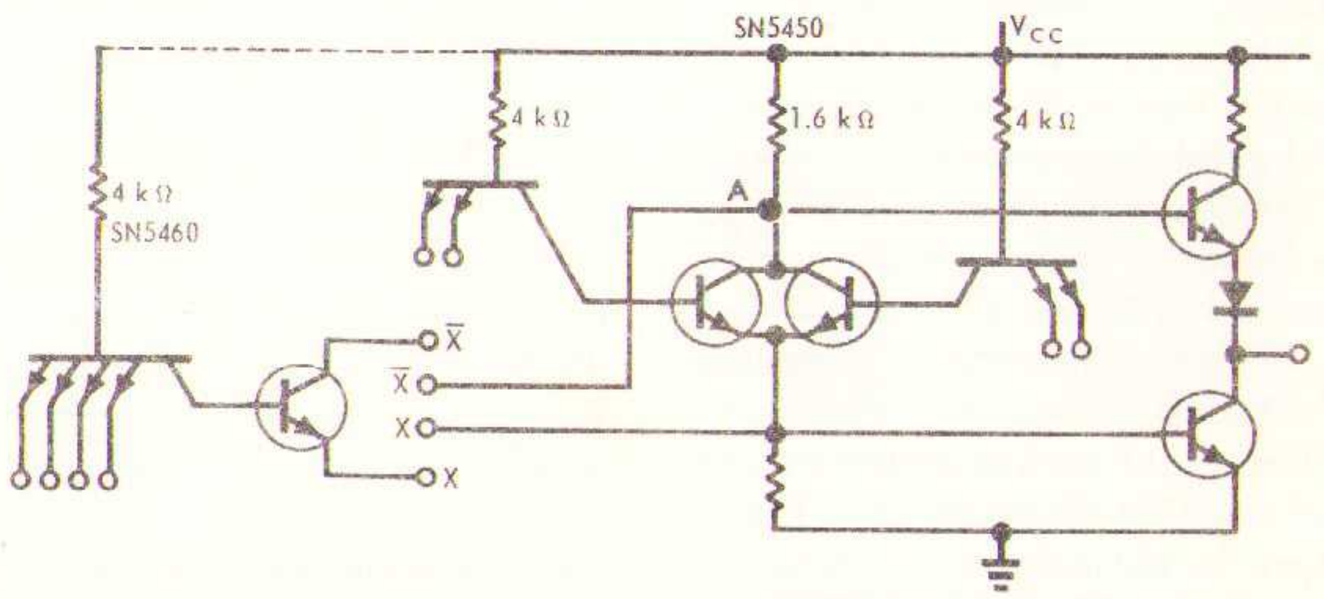


Fig. 3—**Expander gates add stray capacitance** at point A. This accounts for longer rise time when expanders are used.

Taking the average of these two

$$\frac{\Delta V}{\Delta T} = 1.46 \text{ ns/pF}$$

If the rate of rise is 1.46 ns/pF from 0.4 to 2.0V, the increased t_{pd1} measured as the increased time from 0.4 to 1.5V should be:

$$\Delta t_{pd1} = \left(\frac{1.5 - 0.4}{2.0 - 0.4}\right) 1.46 \text{ ns/pF}$$

$$= 1.0 \text{ ns/pF}$$

This figure correlates closely with observed facts.

The same procedure can yield the increase in t_{pd0}. However, the situation is not quite as concise, since the stray capacitance discharges through the wired-OR transistors and the V_{BE} of the output stage. This path has a lower but less precise impedance. Test data show that t_{pd0} increases somewhat less than t_{pd1}, but the 1-ns/pF value should be used for safety.

Solution: Where increased delay is marginal in a system, t_r can be reduced by a factor of 2 by connecting a 1.6k resistor from $\bar{X}$ to V_{CC}, **Fig. 3**. There is no data-sheet guarantee that this connection will work under dc conditions since the I_{ON} test is made with the expander collector open and base current only is measured. If one can assume a minimum h_{FE} of 10 for this device, then the collector current should be sufficient to drive the equivalent 800Ω load. Further reduction of the resistance should not be attempted. For further increases in speed, the SN54H AOI gates and expanders may be substituted.

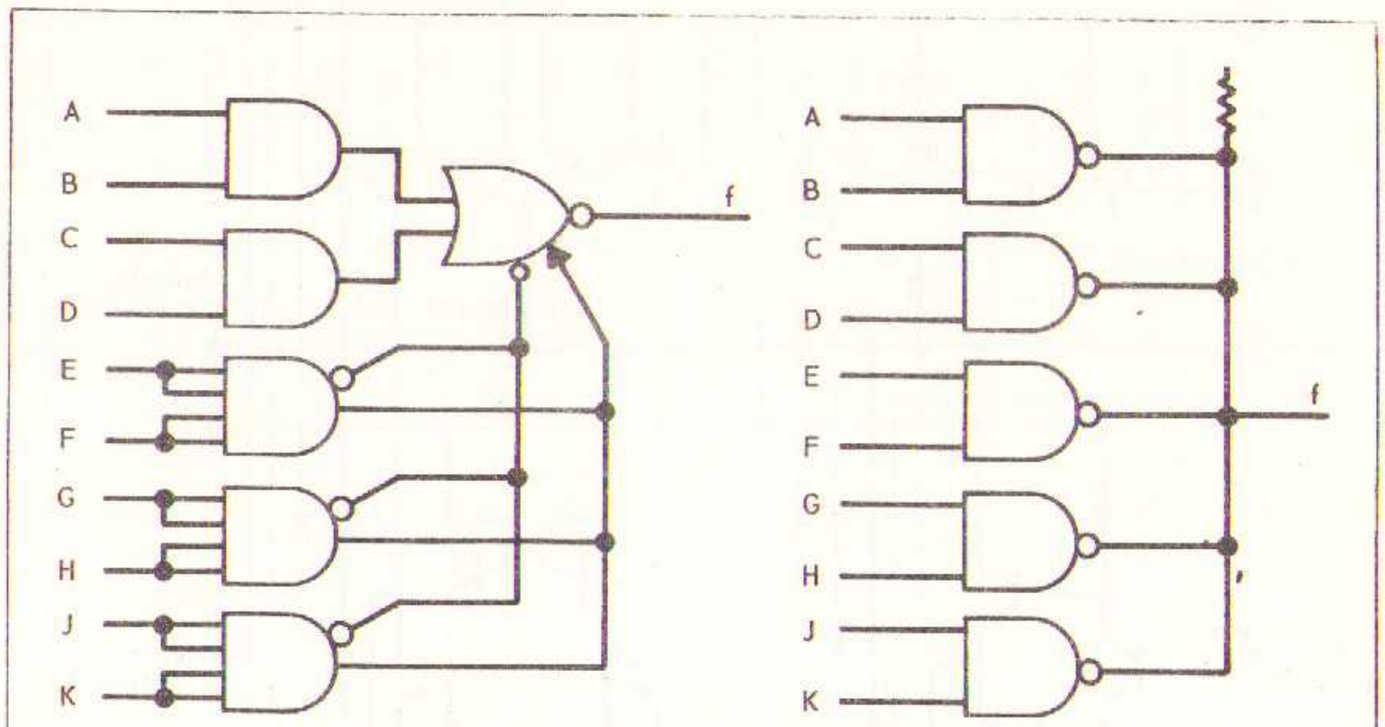


Fig. 4—**One solution is to explore** other implementations of function that avoid use of expander gates.

Alternate implementations may be explored, such as the circuit of **Fig. 4b**, which performs the same logic as **Fig. 4a**. The same analysis holds for the SN7400 series. □

8-Bit Serial Register Shifts Unpredictably

Problem: An 8-bit shift register (SN7491A) transfers all of its stored data to the output on a single clock pulse. At times no clocking seems to occur at all.

Investigation: The shift register in question is an eight-stage serial-in/serial-out shift register. Its R-S flip-flops are similar to the J-K flip-flops in the SN7490 series 4-bit counters. Design of this register is simple, since only the final output, initial inputs and clock line ever see external connections. The devices are level triggered. If only one clock excursion takes place, only one shift should occur. There is no specification on the data or clock inputs other than the "0" and "1" levels. Data entered on the falling edge of the clock shift on the next rise of the clock. The inverted clock scheme is caused by an internal inverting amplifier that is included in the register to reduce the 16-unit clock line load to one unit load.

Deduction: Since it has been shown possible for logic gates to oscillate (see earlier article, "Circuits Timed from 60 Hz Trigger Falsely") it also should be possible for the inverting amplifier to become unstable, because the circuits are similar. (Compare the clock input and gate circuits in **Fig. 1**.) Amplifier oscillation would result in effectively multiple-clocking the register.

Analysis: Since clock waveform characteristics are not defined, it might be assumed that slowly varying clock signals are satisfactory. They are, but only if instability does not occur

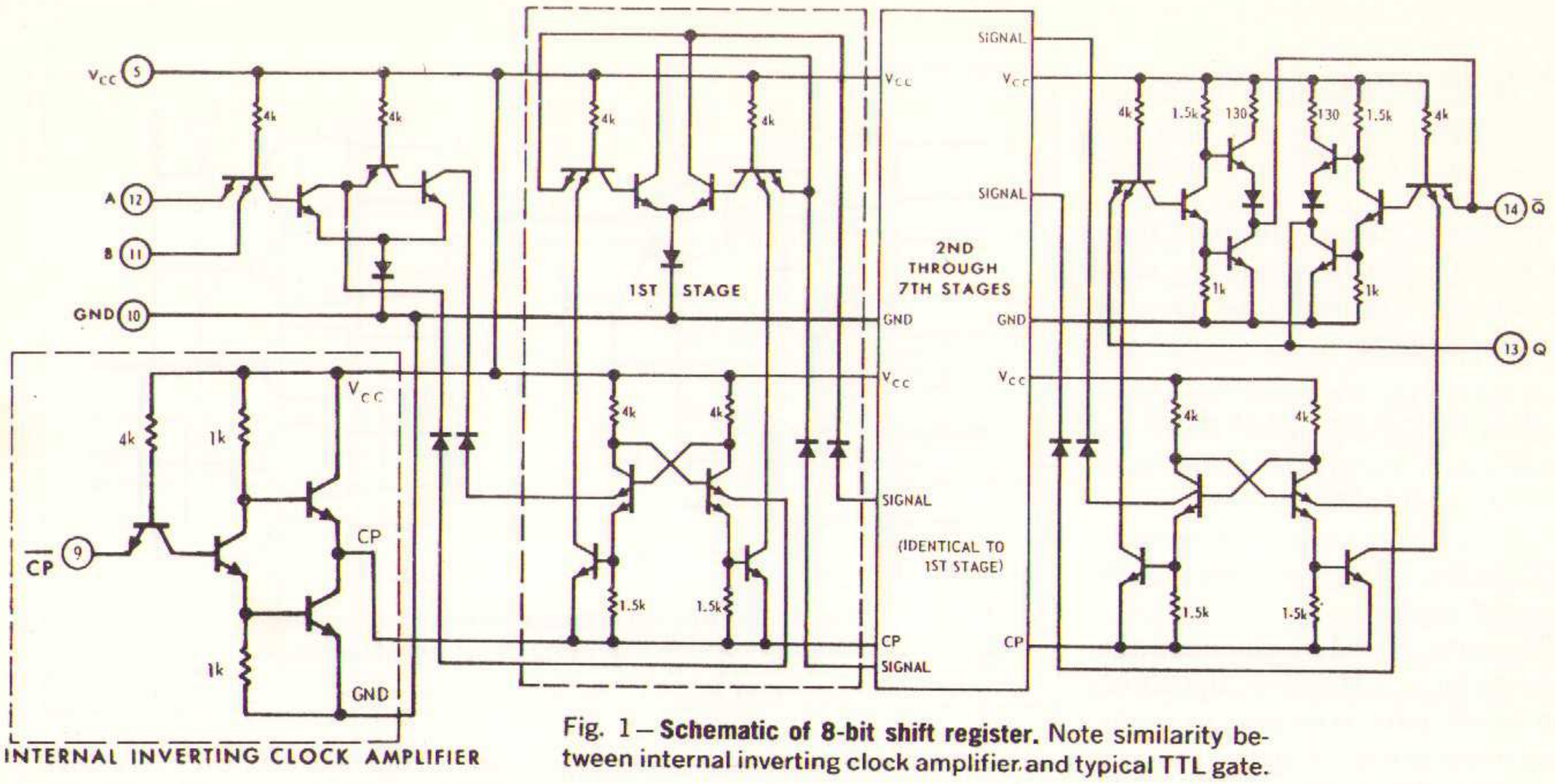


Fig. 1—**Schematic of 8-bit shift register.** Note similarity between internal inverting clock amplifier and typical TTL gate.

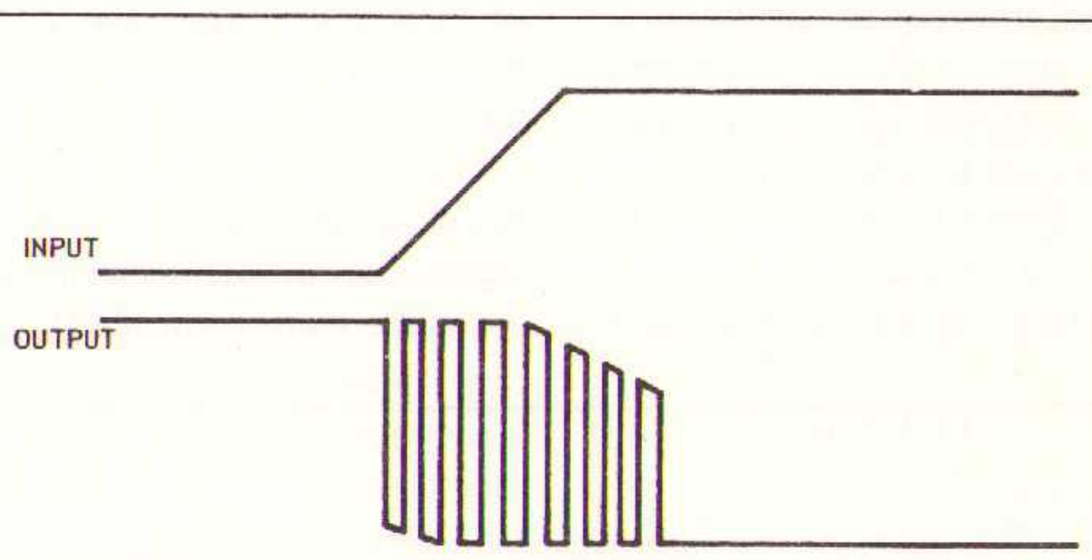


Fig. 2—**With slow-rise external clock,** internal clock amplifier can exhibit a transient unstable condition.

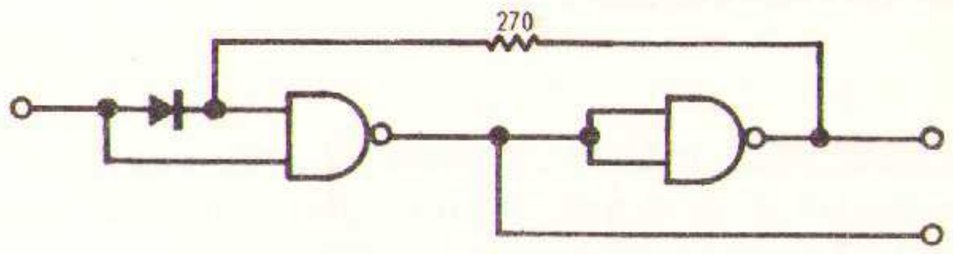


Fig. 3—**Schmitt trigger** with TTL gates will eliminate clock amplifier instability.

while the amplifier is within its active region. If instability does occur, the waveform on the internal flip-flop clock line will be similar to **Fig. 2**.

The troublesome registers were found to be driven by clock pulses with ≈ 1-ms rise and fall times. **Solution:** Shaping external clock pulses with a Schmitt trigger circuit (**Fig. 3**) eliminated the problem. As in the referenced case of the unstable gates, the recommended rise time is ≦ 1 μs. This criterion should be applied to all devices with internal inverting gates, such as the SN7494, SN7495 and SN7496. ▭

O V E R Z I C H T U I T W I S S E L B A R E T T L G E Ï N T E G R E E R D E S C H A K E L I N G E N

Onderstaande typen geïntegreerde schakelingen zijn volkomen uitwisselbaar. Wij wijzen er wel op, dat bij verschillende fabrikanten kleine verschillen in de technische gegevens voorkomen. Veelal hebben deze betrekkelijk weinig invloed op Uw ontwerp. Tevens wijzen wij erop, dat de meeste fabrikanten hun reeks nog aan het uitbreiden zijn, waardoor deze lijst niet als volledig kan worden beschouwd.

AEG	AMPEREX	FAIRCHILD		FERRANTI	ITT	MOTOROLA	NSC	PHILIPS	SESCOSEM	SIEMENS	SIGNETICS		SPRAGUE	TI	TRANSITRON
FLH101	FJH131	9002	U6A740059X	ZN7400E	9002	MC7400P	DM8000N	FJH131	SFC400E	FLH101	N7400A	N8480A	US7400A	SN7400N	TG7400E
-	FJH231	-	U6A740159X	ZN7401E	-	MC7401P	DM8001N	FJH231	-	FLH201	N7401A	N8881A	US7401A	SN7401N	TG7401E
FLH191	FJH221	-	U6A740259X	ZN7402E	-	MC7402P	DM8002N	FJH221	SFC402E	FLH191	N7402A	-	US7402A	SN7402N	TG7402E
-	-	-	U6A740359X	-	-	-	DM8003N	-	-	-	-	-	US7403A	SN7403N	-
-	-	-	U6A740459X	ZN7404E	9016	MC7404P	DM8004N	FJH241	SFC404E	-	-	N8490A	US7404A	SN7404N	TH7404E
FLH111	FJH121	9003	U6A741059X	ZN7410E	9003	MC7410P	DM8010N	FJH121	SFC410E	FLH111	N7410A	N8470A	US7410A	SN7410N	TG7410E
FLH121	FJH111	9004	U6A742059X	ZN7420E	9004	MC7420P	DM8020N	FJH111	SFC420E	FLH121	N7420A	-	US7420A	SN7420N	TG7420E
FLH131	FJH101	-	U6A743059X	ZN7430E	-	MC7430P	DM8030N	FJH101	SFC43CE	FLH131	N7430A	N8808A	US7430A	SN7430N	TG7430E
FLH141	FJH141	9009	U6A744059X	ZN7440E	9009	MC7440P	DM8040N	FJH141	SFC44CE	FLH141	N7440A	N8455A	US7440A	SN7440N	TG7440E
-	FJL101	-	U6B744159X	ZN7441E	-	-	DM8840N	-	SFC441E	-	N7441B	-	US7441B	SN7441AN	TD7441AE
-	-	-	-	-	-	-	DM8842N	-	-	-	-	-	-	SN7442N	-
FLH151	FJH151	9005	U6A745059X	ZN7450E	9005	MC7450P	DM8050N	FJH151	SFC450E	FLH151	N7450A	N8840A	US7450A	SN7450N	TG7450E
-	FJH161	-	U6A745159X	ZN7451E	-	MC7451P	DM8051N	FJH161	SFC451E	FLH161	N7451A	-	US7451A	SN7451N	TG7451E
FLH171	FJH171	-	U6A745359X	ZN7453E	-	MC7453P	DM8053N	FJH171	SFC453E	FLH171	N7453A	-	US7453A	SN7453N	TG7453E
-	FJH181	-	U6A745459X	ZN7454E	-	MC7454P	DM8054N	FJH181	SFC454E	FLH181	N7454A	-	US7454A	SN7454N	TG7454E
FLY101	FJY101	9006	U6A746059X	ZN7460E	9006	MC7460P	DM8060N	FJY101	SFC460E	FLY101	N7460A	N8806A	US7460A	SN7460N	TG7460E
FLJ111	FJJ111	-	U6A747259X	ZN7472E	-	MC7472P	DM8540N	FJJ111	SFC472E	FLJ111	N7472A	-	US7472A	SN7472N	TF7472E
FLJ121	FJJ121	-	U6A747359X	ZN7473E	-	MC7473P	DM8501N	FJJ121	SFC473E	FLJ121	N7473A	-	US7473A	SN7473N	TF7473E
FLJ141	FJJ131	-	U6A747459X	ZN7474E	-	MC7474P	DM8510N	FJJ131	SFC474E	FLJ141	N7474A	N8828A	US7474A	SN7474N	TF7474E
FLJ151	FJJ181	-	U6A747559X	ZN7475E	-	MC7475P	DM8550N	FJJ181	SFC475E	FLJ151	N7475B	N8275B	US7475B	SN7475N	TL7475E
FLJ131	FJJ191	-	U6A747659X	ZN7476E	-	MC7476P	DM8500N	FJJ191	SFC476E	FLJ131	N7476B	-	US7476B	SN7475N	TF7476E
-	-	-	-	-	-	-	DM8283N	-	-	-	-	-	US7483B	SN7483N	TA7483E
-	-	-	-	-	-	-	DM8086N	-	SFC486E	-	-	-	-	SN7486N	-
FLJ161	FJJ141	-	U6A749059X	-	-	-	DM8530N	FJJ141	SFC490E	FLJ161	-	-	US7490A	SN7490N	TC7490E
-	FJJ251	-	U6A749259X	-	-	-	DM8532N	FJJ251	SFC492E	-	-	-	US7492A	SN7490N	TC7492E
-	FJJ211	-	U6A749359X	-	-	MC7493P	DM8533N	FJJ211	SFC493E	-	-	-	US7493A	SN7493N	TC7493E

Wordt U overstelpt met materialen, die U door gebrek aan technische gegevens niet kunt of durft te gebruiken?? Ons leveringsprogramma is opgebouwd met materialen, welke worden gefabriceerd door fabrikanten met een internationale bekendheid; achter elk produkt staat, behalve de fabrikant, een datasheet met alle technische gegevens, waarvan inmiddels een gedeelte in deze uitgave "Technische Documentatie" is opgenomen. In een van de komende nummers worden de nieuw aan het leveringsprogramma toegevoegde TTL IC's besproken, alsmede de technische gegevens van de verdere halfgeleiders.